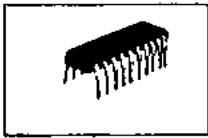




No. 1190 A

LC7132



C MOS LSI
PLL FREQUENCY SYNTHESIZER LSI
FOR 27MHZ CB TRANSCEIVERS

Use

PLL frequency synthesizer LSI for 27MHz CB transceivers (U.S. standard).

Functions, features

1. Built-in high speed programmable divider for direct PLL system.
2. Doubled-frequency of VCO applicable as transmitting frequency carrier.
3. PLL out-of-lock output available to inhibit transmission.
4. Instantaneous call capability of channel 9.
5. Built-in detecting circuit of mis-program.
6. Built-in amplifier for crystal oscillator.
7. Built-in amplifier for active low-pass filter.
8. 7-segment code channel selection. (allowable voltage 15V)

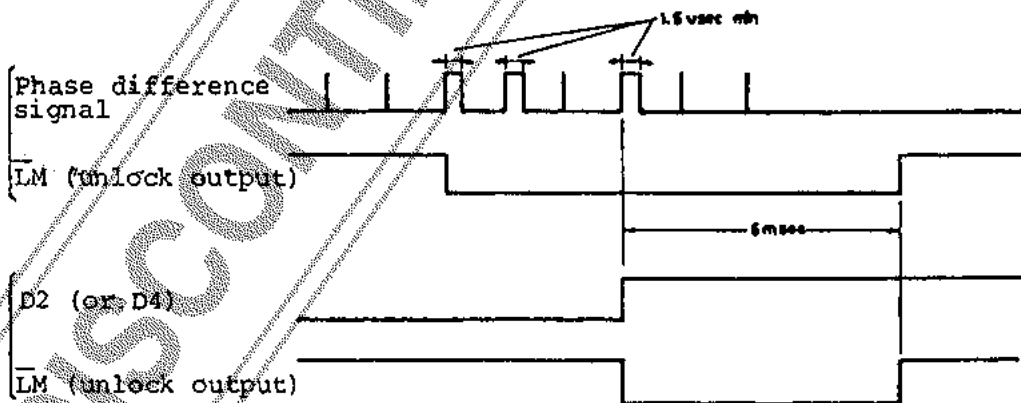
Description of functions

Digital Out-of-Lock Output

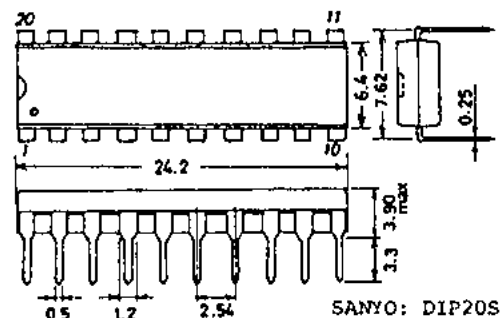
In direct PLL system, phase difference signal's pulse width at channel change is too narrow, so it is difficult to get out-of-lock signal from phase detector in the way of using C,R components externally.

LC7132 makes it possible to output the out-of-lock signal to have digital discriminate-expander of the pulse from phase detector internally (Detects the phase difference signal over 1.6 μ s pulse width, and makes it expand to 6ms output pulse).

And also LC7132 outputs the out-of-lock signal when the phase difference signal is within 1.6 μ s to have the detector of channel change input.



Case Outline
3021B-D20S1C
(unit:mm)



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Instantaneous call of channel 9 and recourse against miscode.

.Setting CH9 at "H" level causes channel 9 to be selected.

.Inputting miscode to D1 to D8 causes channel 19 to occur.

.The following table shows the transmitting/receiving channel corresponding to the combination of D1 to D8 and CH9.

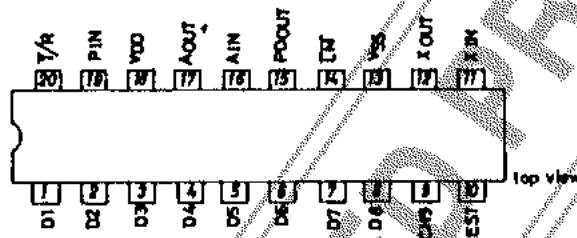
Input		Output
Data of D1 to D8	CH9	Channel
Normal code	0	Channel depending on D1 to D8
	1	Channel 9
Error program	0	Channel 19
	1	Chanel 9

1 : "H" level
0 : "L" level

Built-in amplifier for active low-pass filter

In direct PLL system, active low-pass filter is more available, as lock-up-time of PLL using active low-pass filter is shorter than the one using passive low-pass filter. The LC7132 contains an N channel open drain amplifier for active filter in order to make lockup time shorter.

Pin Assignment



Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Value	Unit
Maximum Supply Voltage	VDDmax		-0.3 to +9.0	V
Maximum Input Voltage	VINmax(1)	D1 to D8, CH9	-0.3 to +17	V
	VINmax(2)	Input pins other than above.	-0.3 to VDD+0.3	V
Maximum Output Voltage	VOUT(1)	LM, AOUT, output off	-0.3 to +10.0	
	VOUT(2)	PDOUT, AOUT, output off	-0.3 to VDD+0.3	V
Maximum Output Current	IOUT(1)	LM	0 to 15	mA
	IOUT(2)	AOUT	0 to 2.5	mA
Allowable Power Dissipation	Pdmax	Ta=70°C	300	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C

Parameter	Symbol	Conditions	min	typ	max	unit
Supply Voltage	VDD	Ta=-30 to +70°C	5.0		8.0	V
Output Voltage	VOUT	LM, AOUT, output off	0		9.0	V
Input Amplitude	VIN(1)	XIN, *, fIN(1)=10.25MHz	1.0	0.9VDD		Vp-p
	VIN(2)	PIN, *, fIN(2)=20MHz	1.0	0.9VDD		Vp-p
Input Frequency	fIN(1)	XIN, *, VIN(1)=1.0Vp-p	1.0		10.25	MHz
	fIN(2)	PIN, *, VIN(2)=1.0Vp-p	1.0		20	MHz
Input "H" Level Voltage	VIH(1)	D1 to D8, CH9	0.8VDD		15	V
	VIH(2)	T/R	0.7VDD		VDD	V
Input "L" Level Voltage	VIL(1)	D1 to D8, CH9	0	0.4VDD		V
	VIL(2)	T/R	0	0.3VDD		V

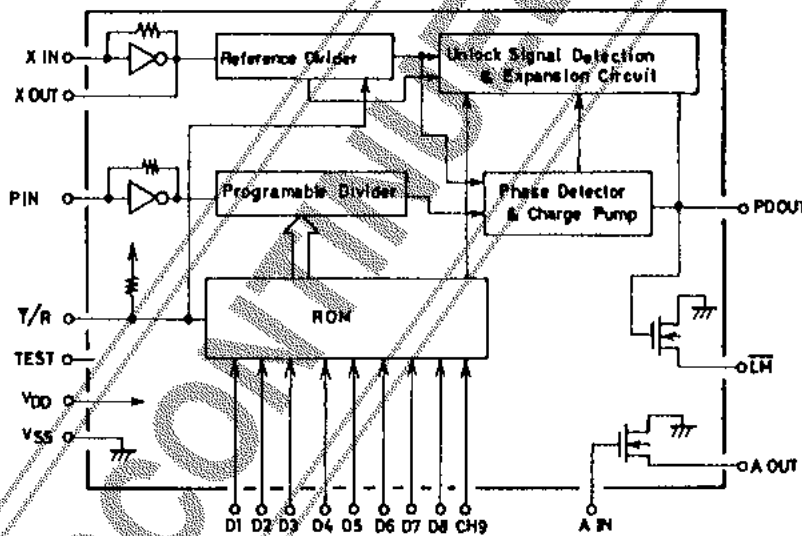
Note * : Sinusoidal wave, capacitive coupling, Ta=-30 to +70°C

Electrical Characteristics at Ta=25°C, VDD=5 to 8V

Parameter	Symbol	Conditions	min	typ	max	unit
Input "H" Level Current	I _{IH} (1)	XIN, PIN VIN=VDD			40	uA
Input "H" Level Current	I _{IH} (2)	D1 to D8, CH9 VIN=15V			5.0	uA
Input "H" Level Current	I _{IH} (3)	AIN VIN=VDD	0.01			nA
Input "L" Level Current	I _{IL} (1)	XIN, PIN VIN=VSS			40	uA
	I _{IL} (2)	D1 to D8, CH9 VIN=VSS			5.0	uA

			min	typ	max	unit
Input "L" Level Current	$I_{IL}(3)$ \bar{T}/R	$V_{IN}=V_{SS}$	40	200	500	μA
	$I_{IL}(4)$ A_{IN}	$V_{IN}=V_{SS}$		0.01		nA
Output "H" Level Voltage	V_{OH} PD_{OUT}	$I_{OUT}=0.3mA$ $V_{DD}-1.0$				V
Output "L" Level Voltage	$V_{OL}(1)$ PD_{OUT}	$I_{OUT}=0.3mA$			1.0	V
	$V_{OL}(2)$ A_{OUT}	$I_{OUT}=0.5mA$			0.3	V
	$V_{OL}(3)$ \bar{LM}	$I_{OUT}=15mA$			1.1	V
Feedback Resistance	$R_F(1)$ X_{IN}			1.0		Mohm
	$R_F(2)$ P_{IN}			0.5		Mohm
Input Threshold Voltage	V_{th}			$1/2V_{DD}$		V
"H" Level 3-State Leak Current	I_{OFFH} PD_{OUT}	$V_{OUT}=V_{DD}$		0.01		nA
"L" Level 3-State Leak Current	I_{OFFL} PD_{OUT}	$V_{OUT}=V_{SS}$		0.01		nA
Input Floating Voltage	$V_{IF}(1)$ \bar{T}/R	Input pins open		$V_{DD}-0.2$		V
Output Off Leak Current	$I_{OFF}(1)$ A_{OUT}	$V_{OUT}=9V$			3.0	μA
	$I_{OFF}(2)$ \bar{LM}	$V_{OUT}=9V$			5.0	μA
Current Dissipation	I_{DD}	$f_{IN}(1)=10.25MHz,$ $f_{IN}(2)=20MHz, V_{IN}(1)=V_{IN}(2)=1.0Vp-p$ $CH9=A_{IN}=V_{SS}, D1 \text{ to } D4, D6 \text{ to } D8=V_{DD}, D5=V_{SS},$ Other pins open, Number of frequency divisions=3254		10	20	mA

Equivalent Circuit and Block Diagram



- D1 to D8 : Program input (7-segment code)
- X IN, X OUT : Amplifier for crystal oscillator
- V DD, V SS : Power Supply
- \bar{LM} : Lock monitor output Lock--open"1", unlock--"0"
- PD OUT : Charge pump output
- A IN, A OUT : Amplifier for low-pass filter
- P IN : Programmable divider input
- \bar{T}/R : Transmission/reception changeover input
 $\bar{T}/R="0"$ ---Transmission $\bar{T}/R="1"$
 $\bar{T}/R="1"$ (or open)---reception
- CH9 : Channel 9 select input
- TEST : LSI test pin (TEST pin:Connected to V SS or open)

