Current Output, Parallel Input, 16-/14-Bit Multiplying DACs with 4-Quadrant Resistors

AD5546/AD5556

FEATURES

- 16-bit resolution
- 14-bit resolution
- 2- or 4-quadrant multiplying DAC
- ±1 LSB DNL
- ±1 LSB INL or ±2 LSB INL
- Operating supply voltage: 2.7 V to 5.5 V
- Low noise: 12 nV/√Hz
- Low power: I_{DD} = 10 µA
- 0.5 µs settling time
- Built-in R_{FB} facilitates current-to-voltage conversion
- Built-in 4-quadrant resistors allow 0 V to –10 V, 0 V to +10 V, or ±10 V outputs
- 2 mA full-scale current ±20%, with V_{REF} = 10 V
- Automotive operating temperature: –40°C to +125°C
- Compact TSSOP-28 package

APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration
- Digital waveform generation

FUNCTIONAL BLOCK DIAGRAM

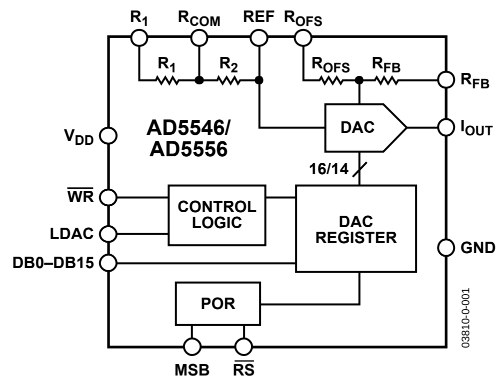

Figure 1. AD5546/AD5556 Simplified Block Diagram

GENERAL DESCRIPTION

The AD5546/AD5556 are precision 16-/14-bit, multiplying, low power, current output, parallel input D/A converters. They operate from a single 2.7 V to 5.5 V supply with ±10 V multiplying references for 4-quadrant outputs. Built-in 4-quadrant resistors facilitate the resistance matching and temperature tracking that minimize the number of components needed for multiquadrant applications. The feedback resistor (R_{FB}) simplifies the I-V conversion with an external buffer. The AD5546/AD5556 are packaged in compact TSSOP-28 packages with operating temperatures from –40°C to +125°C.

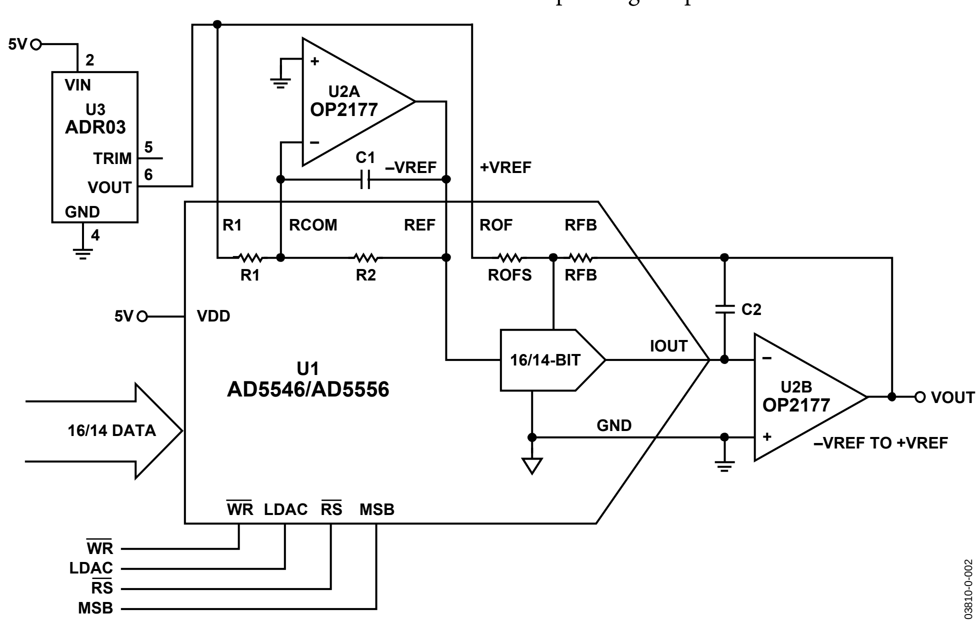

Figure 2. 16-/14-Bit, 4-Quadrant Multiplying DAC with a Minimum of External Components

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

Table 1. Electrical Characteristics. V_{DD} = 2.7 V to 5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = −10 V to 10 V, T_A = full operating temperature range, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[1]						
Resolution	N	AD5546, 1 LSB = $V_{REF}/2^{16}$ = 153 µV at V_{REF} = 10 V		16		Bits
Resolution	N	AD5556, 1 LSB = $V_{REF}/2^{14}$ = 610 µV at V_{REF} = 10 V		14		Bits
Relative Accuracy	INL	Grade: AD5556C			±1	LSB
Relative Accuracy	INL	Grade: AD5546B			±2	LSB
Differential Nonlinearity	DNL	Monotonic			±1	LSB
Output Leakage Current	I_{OUT}	Data = zero scale, T_A = 25°C			10	nA
Output Leakage Current	I_{OUT}	Data = zero scale, T_A = T_A maximum			20	nA
Full-Scale Gain Error	G_{FSE}	Data = full scale		±1	±4	mV
Bipolar Mode Gain Error	G_E	Data = full scale		±1	±4	mV
Bipolar Mode Zero-Scale Error	G_{ZSE}	Data = full scale		±1	±2.5	mV
Full-Scale Tempco	TCV_{FS}			1		ppm/°C
REFERENCE INPUT						
V_{REF} Range	V_{REF}		−18		+18	V
REF Input Resistance	REF		4	5	6	kΩ
R1 and R2 Resistance	R1 and R2		4	5	6	kΩ
R1-to-R2 Mismatch	Δ(R1 to R2)			±0.5	±1.5	Ω
Feedback and Offset Resistance	R_{FB}, R_{OFS}		8	10	12	kΩ
Input Capacitance[2]	C_{REF}			5		pF
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = full scale		2		mA
Output Capacitance	C_{OUT}	Code dependent		200		pF
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	V_{IL}	V_{DD} = 5 V			0.8	V
Logic Input Low Voltage	V_{IL}	V_{DD} = 3 V			0.4	V
Logic Input High Voltage	V_{IH}	V_{DD} = 5 V	2.4			V
Logic Input High Voltage	V_{IH}	V_{DD} = 3 V	2.1			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}				10	pF
INTERFACE TIMING[, 3]						
Data to $\overline{WR}$ Setup Time	t_{DS}	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
Data to $\overline{WR}$ Hold Time	t_{DH}	V_{DD} = 5 V	0			ns
		V_{DD} = 3 V	0			ns
$\overline{WR}$ Pulse Width	$t_{\overline{WR}}$	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
LDAC Pulse Width	t_{LDAC}	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
$\overline{RS}$ Pulse Width	t_{RS}	V_{DD} = 5 V	20			ns
		V_{DD} = 3 V	35			ns
$\overline{WR}$ to LDAC Delay Time	t_{LWD}	V_{DD} = 5 V	0			ns
		V_{DD} = 3 V	0			ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			10	µA
Power Dissipation	P_{DISS}	Logic inputs = 0 V			0.055	mW
Power Supply Sensitivity	P_{SS}	$\Delta V_{DD} = \pm 5\%$			0.003	%/%
AC CHARACTERISTICS[4]						
Output Voltage Settling Time	t_S	To ±0.1% of full scale, data cycles from zero scale to full scale to zero scale		0.5		µs
Reference Multiplying BW	BW	V_{REF} = 5 V p-p, data = full scale		4		MHz
DAC Glitch Impulse	Q	V_{REF} = 0 V, midscale to midscale minus 1		7		nV-s
Multiplying Feedthrough Error	V_{OUT}/V_{REF}	V_{REF} = 100 mV rms, f = 10 kHz		–65		dB
Digital Feedthrough	Q_D	$\overline{WR}$ = 1, LDAC toggles at 1MHz		7		nV-s
Total Harmonic Distortion	THD	V_{REF} = 5 V p-p, data = full-scale, f = 1 KHz		–85		dB
Output Noise Density	e_N	f = 1 kHz, BW = 1 Hz		12		nV/rt Hz

[1] All static performance tests (except I_{OUT}) are performed in a closed-loop system, using an external precision OP97 I-V converter amplifier. The AD554x RFB terminal is tied to the amplifier output. The op amp +IN is grounded and the DAC I_{OUT} is tied to the op amp –IN. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V), and timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD841 I-V converter amplifier.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V, +8 V
R_{FB}, R_{OFS}, R_1, R_{COM}, and REF to GND	−18 V, 18 V
Logic Inputs to GND	−0.3 V, +8 V
$V(I_{OUT})$ to GND	−0.3 V, V_{DD} + 0.3 V
Input Current to Any Pin except Supplies	±50 mA
Thermal Resistance (θ_{JA})	128°C
Maximum Junction Temperature ($T_{J\ MAX}$)	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature:	
Vapor Phase, 60 s	215°C
Infrared, 15 s	220°C
Package Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS

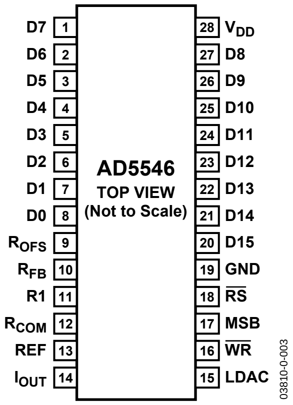

Figure 3.AD5546 Pin Configuration

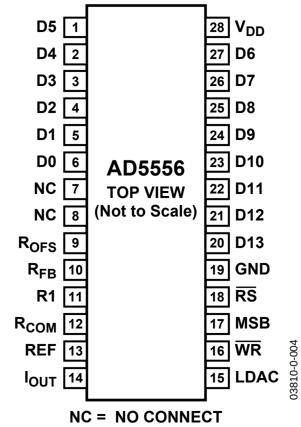

Figure 4. AD5556 Pin Configuration

Table 3. AD5546 Functional Descriptions

Pin No.	Mnemonic	Description
1–8	D7 to D0	Digital Input Data Bits D7 to D0. Signal level must be ≤ V_{DD} + 0.3 V.
9	R_{OFS}	Bipolar Offset Resistor. Accepts up to ±18 V. In 2-quadrant mode ties to R_{FB}. In 4-quadrant mode ties to R1 and external reference.
10	R_{FB}	Internal Matching Feedback Resistor. Connects to the output of an external op amp for I-V conversion.
11	R1	4-Quandrant Resistor R1. In 2-quadrant mode shorts to REF pin. In 4-quadrant mode ties to R_{OFS}.
12	R_{COM}	Center Tap Point of Two 4-Quadrant Resistors, R1 and R2. In 4-quadrant mode, ties to the inverting node of the reference amplifier. In 2-quadrant mode, shorts to REF pin.
13	REF	DAC Reference Input in 2-Quadrant Mode and R2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, this is the reference input with constant input resistance versus code. In 4-quadrant mode, this pin is driven by the external reference amplifier.
14	I_{OUT}	DAC Current Output. Connects to the inverting node of an external op amp for I-V conversion.
15	LDAC	Digital Input Load DAC Control. Signal level must be ≤ V_{DD} + 0.3 V.
16	$\overline{WR}$	Write Control Digital Input in Active Low. Transfers shift-register data to DAC register on rising edge. Signal level must be ≤ V_{DD} + 0.3 V.
17	MSB	Power-On Reset State. MSB = 0 resets at zero scale, MSB = 1 resets at midscale. Signal level must be ≤ V_{DD} + 0.3 V.
18	$\overline{RS}$	Reset in Active Low. Resets to zero scale if MSB = 0, and resets to midscale if MSB = 1. Signal level must be ≤ V_{DD} + 0.3 V.
19	GND	Analog and Digital Grounds.
20–21	D15 to D14	Digital Input Data Bits D15 to D14. Signal level must be ≤ V_{DD} + 0.3 V.
22–27	D13 to D8	Digital Input Data Bits D13 to D8. Signal level must be ≤ V_{DD} + 0.3 V.
28	V_{DD}	Positive Power Supply Input. Specified range of operation: 2.7 V to 5.5 V.

Table 4. AD5556 Functional Descriptions

Pin No.	Mnemonic	Description
1–6	D5 to D0	Digital Input Data Bits D5 to D0. Signal level must be ≤ V_{DD}+0.3 V.
7–8	NC	No Connection. User should not connect anything other than dummy pads on these terminals.
9	R_{OFS}	Bipolar Offset Resistor. Accepts up to ±18 V. In 2-quadrant mode ties to RFB. In 4-quadrant mode ties to R1 and external reference.
10	R_{FB}	Internal Matching Feedback Resistor. Connects to the output of an external op amp for I-V conversion.
11	R1	4-Quandrant Resistor R1. In 2-quadrant mode shorts to REF pin. In 4-quadrant mode ties to R_{OFS}.
12	R_{COM}	Center Tap Point of Two 4-Quadrant Resistors, R1 and R2. In 4-quadrant mode, ties to the inverting node of the reference amplifier. In 2-quadrant mode, shorts to REF pin.
13	REF	DAC Reference Input in 2-Quadrant Mode and R2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, this is the reference input with constant input resistance versus code. In 4-quadrant mode, this pin is driven by the external reference amplifier.
14	I_{OUT}	DAC Current Output. Connects to the inverting node of an external op amp for I-V conversion.

Pin No.	Mnemonic	Description
15	LDAC	Digital Input Load DAC Control. Signal level must be ≤ V_{DD} + 0.3 V.
16	$\overline{\text{WR}}$	Write Control Digital Input in Active Low. Transfers shift-register data to DAC register on rising edge. Signal level must be ≤ V_{DD} + 0.3 V.
17	MSB	Power On Reset State. MSB = 0 resets at zero-scale, MSB = 1 resets at midscale. Signal level must be ≤ V_{DD} + 0.3 V.
18	$\overline{\text{RS}}$	Reset in Active Low. Resets to zero-scale if MSB = 0 and resets to midscale if MSB = 1. Signal level must be ≤ V_{DD} + 0.3 V.
19	GND	Analog and Digital Grounds.
20–27	D13 to D6	Digital Input Data Bits D13 to D6. Signal level must be ≤ V_{DD} + 0.3 V.
28	V_{DD}	Positive power supply input. Specified range of operation: 2.7 V to 5.5 V.

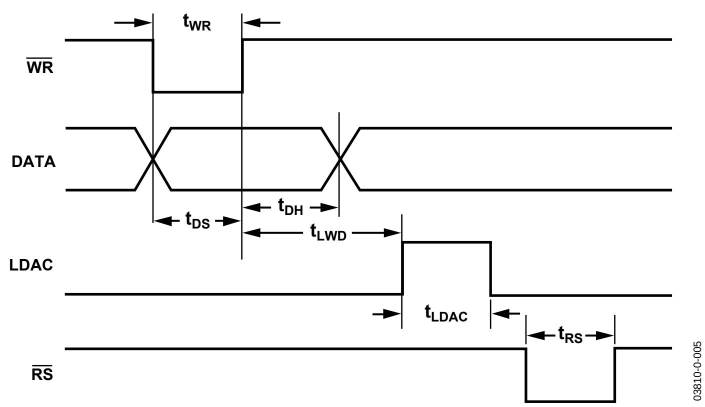

Figure 5. AD5546/AD5556 Timing Diagram

Table 5. AD5546 Parallel Input Data Format

	MSB															LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 6. AD5556 Parallel Input Data Format

	MSB													LSB
Bit Position	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 7. Control Inputs

$\overline{\text{RS}}$	$\overline{\text{WR}}$	LDAC	Register Operation
0	X	X	Reset output to 0, with MSB pin = 0. Midscale with MSB pin = 1.
1	0	0	Load input register with data bits.
1	1	1	Load DAC register with the contents of the input register.
1	0	1	Input and DAC registers are transparent.
1			When LDAC and $\overline{\text{WR}}$ are tied together and programmed as a pulse, the data bits are loaded into the input register on the falling edge of the pulse, and then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

TYPICAL PERFORMANCE CHARACTERISTICS

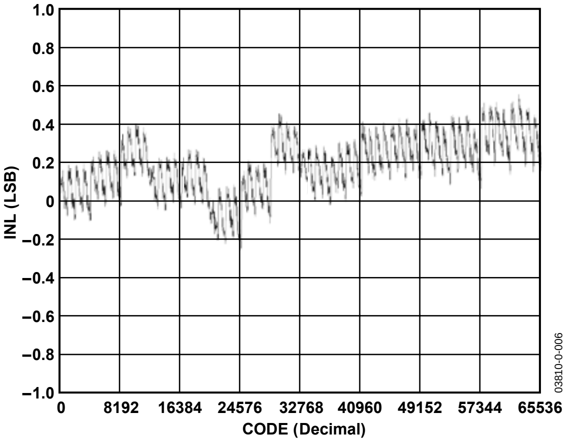

Figure 6. AD5546 Integral Nonlinearity Error

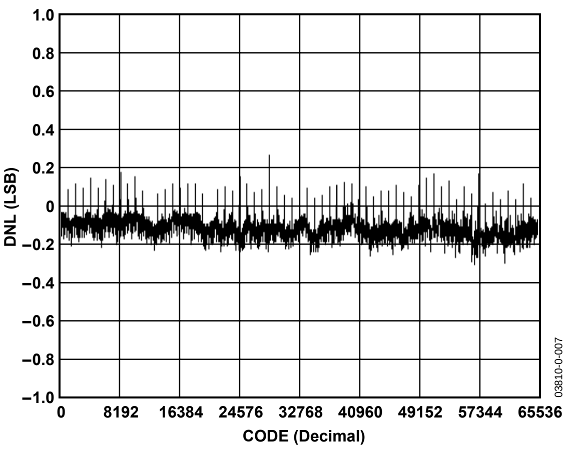

Figure 7. AD5546 Differential Nonlinearity Error

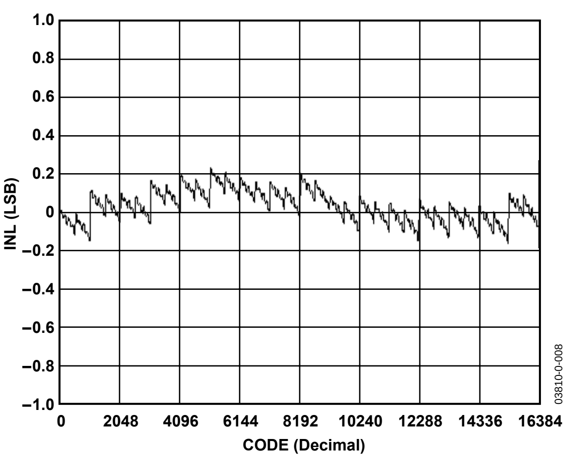

Figure 8. AD5556 Integral Nonlinearity Error

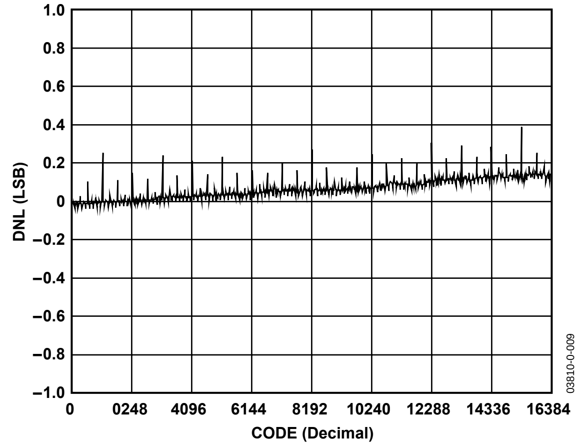

Figure 9. AD5556 Differential Nonlinearity Error

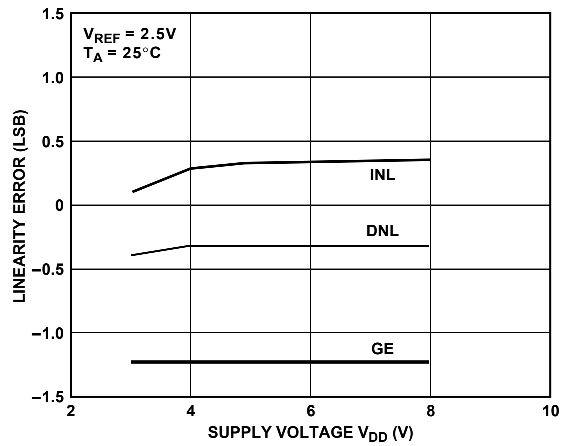

Figure 10. Linearity Error vs. V_{DD}

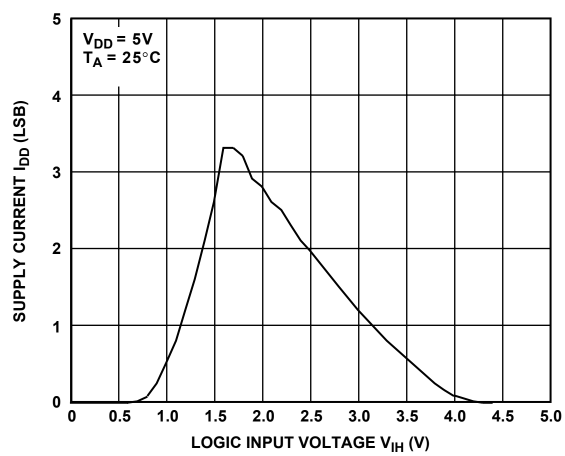

Figure 11. Supply Current vs. Logic Input Voltage

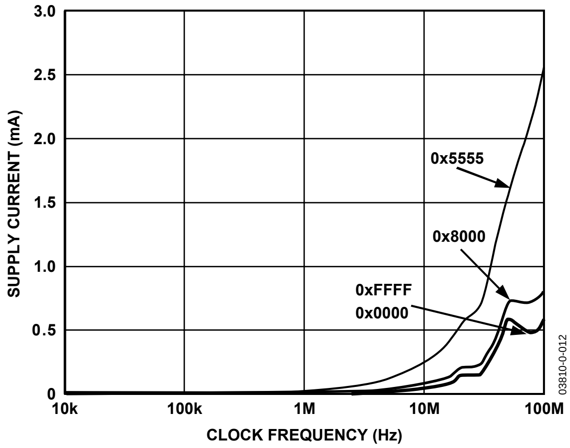

Figure 12. AD5546 Supply Current vs. Clock Frequency

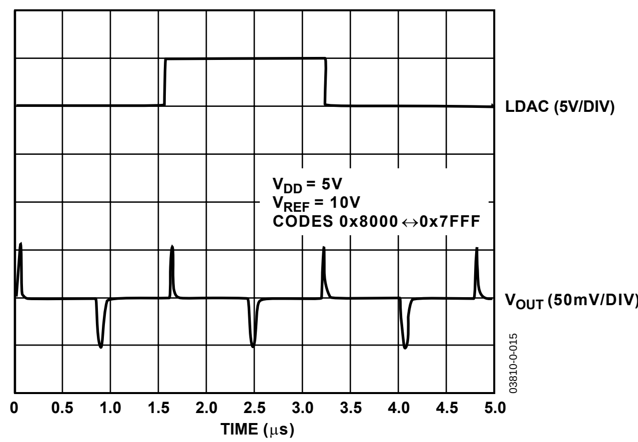

Figure 15. AD5546 Midscale Transition and Digital Feedthrough

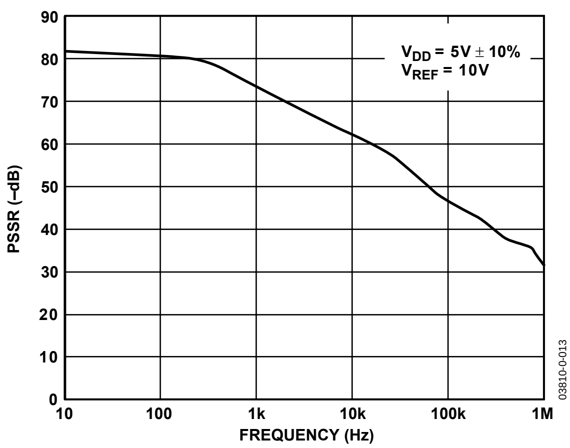

Figure 13. Power Supply Rejection Ratio vs. Frequency

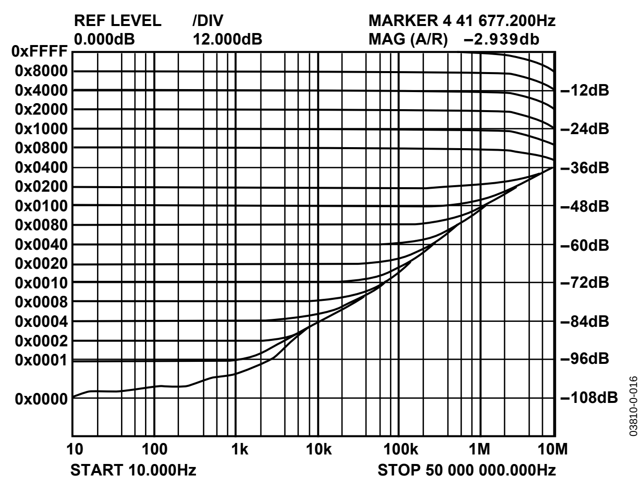

Figure 16. AD5546 Unipolar Reference Multiplying Bandwidth

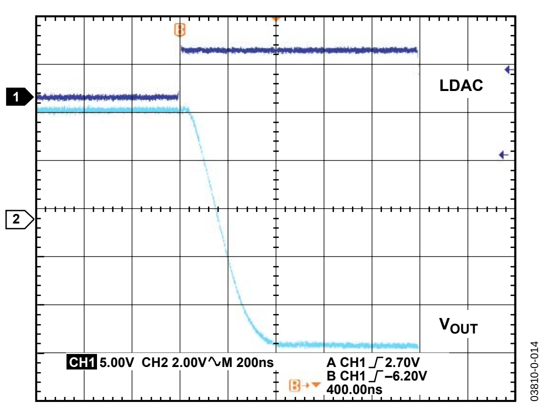

Figure 14. Settling Time from Full Scale to Zero Scale

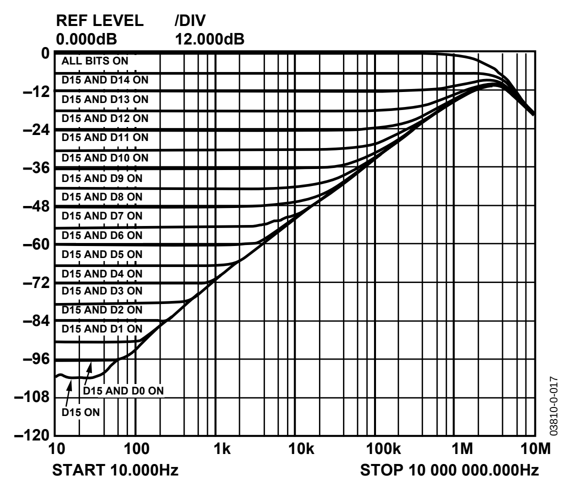

Figure 17. AD5546 Bipolar Reference Multiplying Bandwidth (Codes from Midscale to Full Scale)

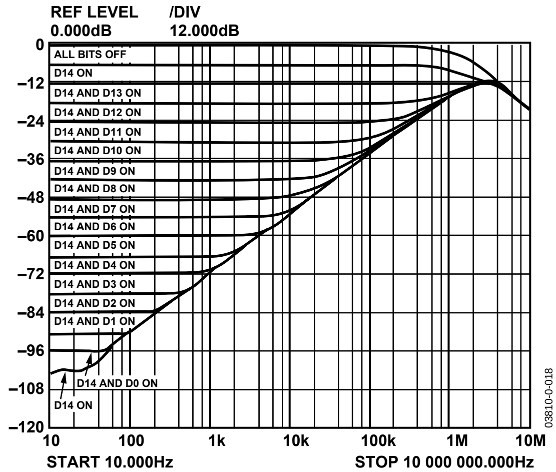

Figure 18. AD5546 Bipolar Reference Multiplying Bandwidth (Codes from Midscale to Zero Scale)

CIRCUIT OPERATION

D/A CONVERTER SECTION

The AD5546/AD5556 are 16-/14-bit multiplying, current output, and parallel input DACs. The devices operate from a single 2.7 V to 5.5 V supply, and provide both unipolar 0 V to $-V_{REF}$, or 0 V to $+V_{REF}$, and bipolar $\pm V_{REF}$ output ranges from a −18 V to +18 V reference. In addition to the precision conversion R_{FB} commonly found in current output DACs, there are three additional precision resistors for 4-quadrant bipolar applications.

The AD5546/AD5556 consist of two groups of precision R-2R ladders, which make up the 12/10 LSBs, respectively. Furthermore, the four MSBs are decoded into 15 segments of resistor value 2R. Figure 19 shows the architecture of the 16-bit AD5546. Each of the 16 segments in the R-2R ladder carries an equally weighted current of one-sixteenth of full scale. The feedback resistor, R_{FB}, and 4-quadrant resistor, R_{OFS}, have values of 10 kΩ. Each 4-quadrant resistor, R1 and R2, equals 5 kΩ. In 4-quadrant operation, R1, R2, and an external op amp work together to invert the reference voltage and apply it to the REF input. With R_{OFS} and R_{FB} connected as shown in Figure 2, the output can swing from $-V_{REF}$ to $+V_{REF}$.

The reference voltage inputs exhibit a constant input resistance of 5 kΩ ±20%. The DAC output, I_{OUT}, impedance is code dependent. External amplifier choice should take into account the variation of the AD5546/AD5556 output impedance. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. To maintain good analog performance, it is recommended to bypass the power supply with a 0.01 μF to 0.1 μF ceramic or chip capacitor in parallel with a 1 μF tantulum capacitor. Also, to minimize gain error, PCB metal traces between V_{REF} and R_{FB} should match.

Every code change of the DAC corresponds to a step function; gain peaking at each output step may occur if the op amp has limited GBP and excessive parasitic capacitance present at the op amp inverting node. A compensation capacitor, therefore, may be needed between the I-V op amp inverting and output nodes to smooth the step transition. Such a compensation capacitor should be found empirically, but a 20 pF capacitor is generally adequate for the compensation.

The V_{DD} power is used primarily by the internal logic and to drive the DAC switches. Note that the output precision degrades if the operating voltage falls below the specified voltage. Users should also avoid using switching regulators because device power supply rejection degrades at higher frequencies.

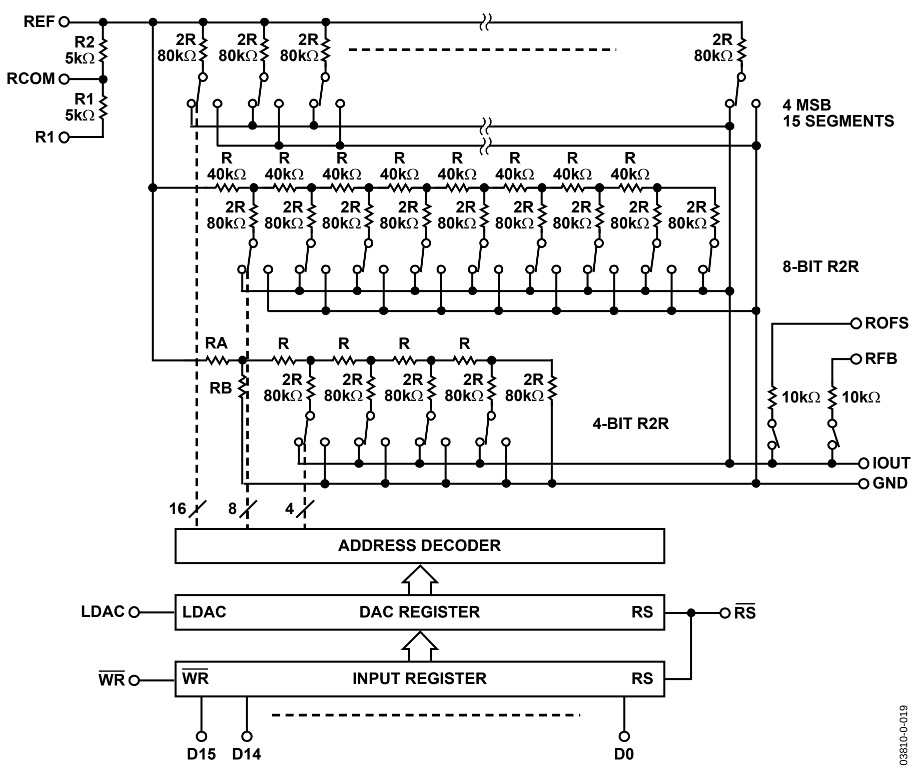

Figure 19. 16-Bit AD5546 Equivalent R-2R DAC Circuit with Digital Section

DIGITAL SECTION

The AD5546/AD5556 have 16-/14-bit parallel inputs. The devices are double-buffered with 16-/14-bit registers. The double-buffered feature allows the update of several AD5546/AD5556 simultaneously. For AD5546, the input register is loaded directly from a 16-bit controller bus when the $\overline{WR}$ pin is brought low. The DAC register is updated with data from the input register when LDAC is brought high. Updating the DAC register updates the DAC output with the new data (see Figure 19). To make both registers transparent, tie $\overline{WR}$ low and LDAC high. The asynchronous $\overline{RS}$ pin resets the part to zero scale if MSB pin = 0, and midscale if MSB pin = 1.

ESD PROTECTION CIRCUITS

All logic input pins contain back-biased ESD protection Zeners connected to ground (GND) and V_{DD}, as shown in Figure 20. As a result, the voltage level of the logic input should not be greater than the supply voltage.

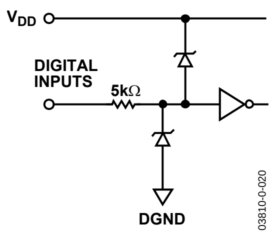

Figure 20. Equivalent ESD Protection Circuits

AMPLIFIER SELECTION

In addition to offset voltage, the bias current is important in op amp selection for precision current output DACs. An input bias current of 30 nA in the op amp contributes to 1 LSB in the AD5546's full-scale error. Op amps OP1177 and AD8628 are good candidates for the I-V conversion.

REFERENCE SELECTION

The initial accuracy and the rated output of the voltage reference determine the full span adjustment. The initial accuracy is usually a secondary concern in precision, as it can be trimmed. Figure 25 shows an example of a trimming circuit. The zero scale error can also be minimized by standard op amp nulling techniques.

The voltage reference temperature coefficient and long-term drift are primary considerations. For example, a 5 V reference with a TC of 5 ppm/°C means that the output changes by 25 µV per degree Celsius. As a result, the reference that operates at 55°C contributes an additional 750 µV full-scale error.

Similarly, the same 5 V reference with a ±50 ppm long-term drift means that the output may change by ±250 µV over time. Therefore, it is practical to calibrate a system periodically to maintain its optimum precision.

APPLICATIONS

UNIPOLAR MODE

2-Quadrant Multiplying Mode, V_{OUT} = 0 V to $-V_{REF}$

The AD5546/AD5556 DAC architecture uses a current-steering R-2R ladder design that requires an external reference and op amp to convert the unipolar mode of output voltage to

$$V_{OUT} = -V_{REF} \times D/65{,}536 \quad \text{(AD5546)} \tag{1}$$

$$V_{OUT} = -V_{REF} \times D/16{,}384 \quad \text{(AD5556)} \tag{2}$$

where D is the decimal equivalent of the input code.

The output voltage polarity is opposite to the V_{REF} polarity in this case (see Figure 21). Table 8 shows the negative output versus code for the AD5546.

Table 8. AD5546 Unipolar Mode Negative Output vs. Code

D in Binary	V_{OUT} (V)
1111 1111 1111 1111	$-V_{REF}$(65,535/65,536)
1000 0000 0000 0000	$-V_{REF}$/2
0000 0000 0000 0001	$-V_{REF}$(1/65,536)
0000 0000 0000 0000	0

2-Quadrant Multiplying Mode, V_{OUT} = 0 V to $+V_{REF}$

The AD5546/AD5556 are designed to operate with either positive or negative reference voltages. As a result, positive output can be achieved with an additional op amp, (see Figure 22), and the output becomes

$$V_{OUT} = +V_{REF} \times D/65{,}536 \quad \text{(AD5546)} \tag{3}$$

$$V_{OUT} = +V_{REF} \times D/16{,}384 \quad \text{(AD5556)} \tag{4}$$

Table 9 shows the positive output versus code for the AD5546.

Table 9. AD5546 Unipolar Mode Positive Output vs. Code

D in Binary	V_{OUT} (V)
1111 1111 1111 1111	$+V_{REF}$(65,535/65,536)
1000 0000 0000 0000	$+V_{REF}$/2
0000 0000 0000 0001	$+V_{REF}$(1/65,536)
0000 0000 0000 0000	0

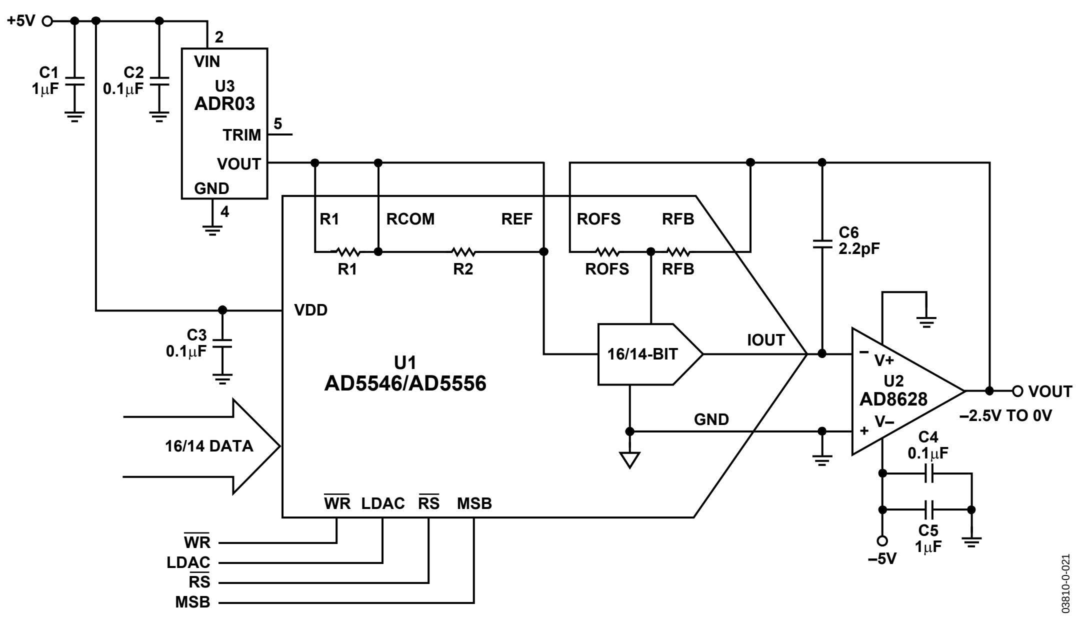

Figure 21. Unipolar 2-Quadrant Multiplying Mode, V_{OUT} = 0 to $-V_{REF}$

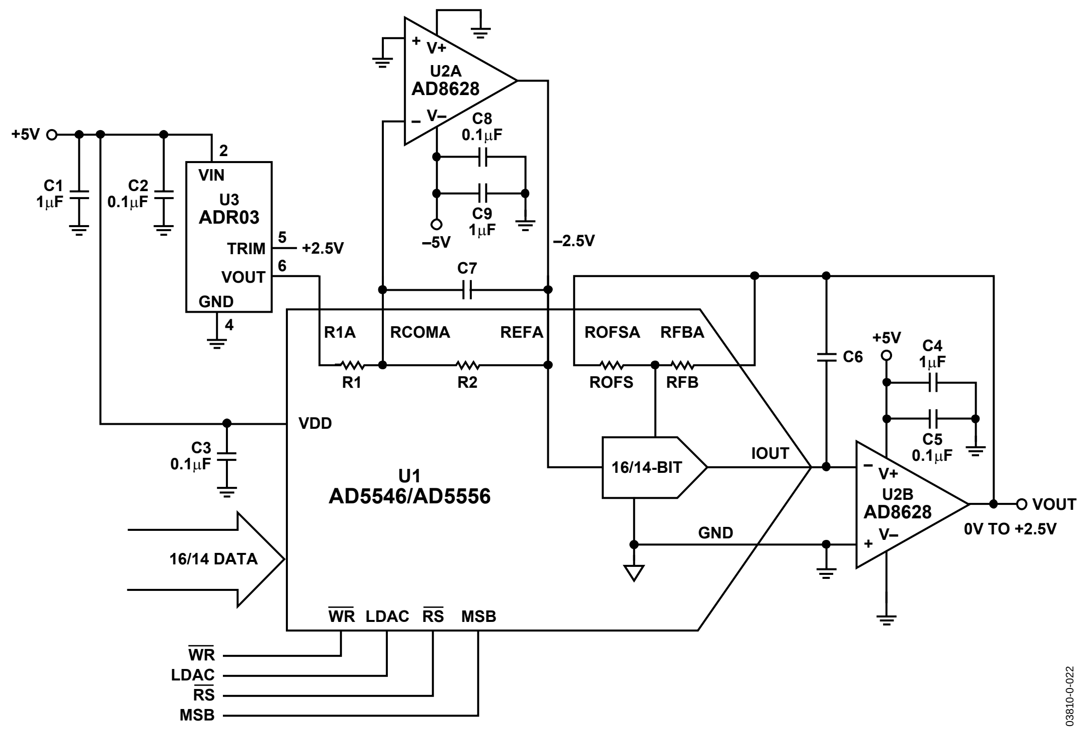

Figure 22. Unipolar 2-Quadrant Multiplying Mode, V_{OUT} = 0 to +V_{REF}

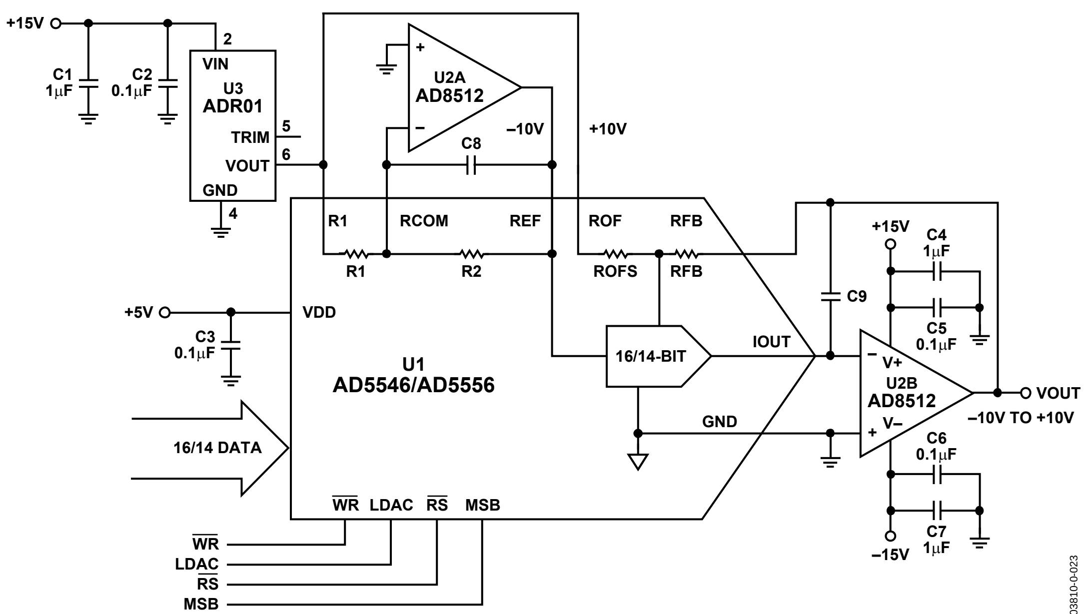

Figure 23. 4-Quadrant Multiplying Mode, V_{OUT} = –V_{REF} to +V_{REF}

BIPOLAR MODE

4-Quadrant Multiplying Mode, V_{OUT} = –V_{REF} to +V_{REF}

The AD5546/AD5556 contain on-chip all the 4-quadrant resistors necessary for the precision bipolar multiplying operation. Such a feature minimizes the number of exponent components to only a voltage reference, dual op amp, and compensation capacitor (see Figure 23). For example, with a 10 V reference, the circuit yields a precision, bipolar –10 V to +10 V output.

$$V_{OUT} = (D/32768 - 1) \times V_{REF} \quad \text{(AD5546)} \tag{5}$$

$$V_{OUT} = (D/16384 - 1) \times V_{REF} \quad \text{(AD5556)} \tag{6}$$

Table 10 shows some of the results for the 16-bit AD5546.

Table 10. AD5546 Output vs. Code

D in Binary	V_{OUT}
1111 1111 1111 1111	$+V_{REF}(32,767/32,768)$
1000 0000 0000 0001	$+V_{REF}(1/32,768)$
1000 0000 0000 0000	0
0111 1111 1111 1111	$-V_{REF}(1/32,768)$
0000 0000 0000 0000	$-V_{REF}$

AC REFERENCE SIGNAL ATTENUATOR

Besides handling digital waveforms decoded from parallel input data, the AD5546/AD5556 handle equally well low frequency ac reference signals for signal attenuation, channel equalization, and waveform generation applications. The maximum signal range can be up to ±18 V (see Figure 24).

SYSTEM CALIBRATION

The initial accuracy of the system can be adjusted by trimming the voltage reference ADR0x with a digital potentiometer (see Figure 25). The AD5170 provides an OTP (one time programmable), 8-bit adjustment that is ideal and reliable for such calibration. ADI's OTP digital potentiometer comes with programmable software that simplifies the factory calibration process.

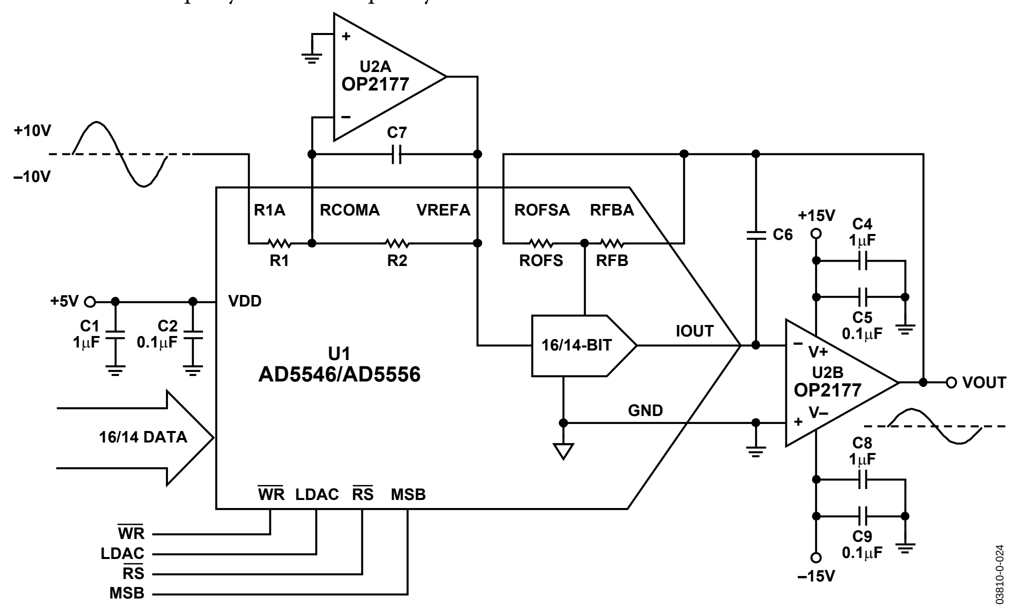

Figure 24. Signal Attenuator with AC Reference

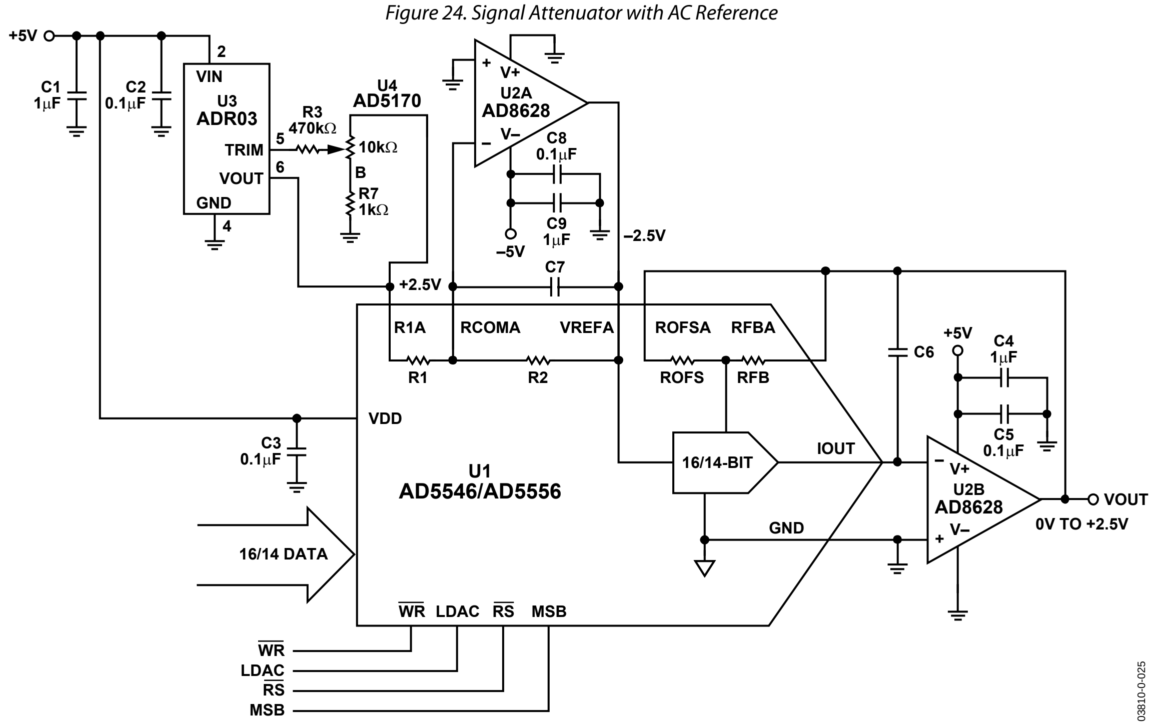

Figure 25. Full Span Calibration

OUTLINE DIMENSIONS

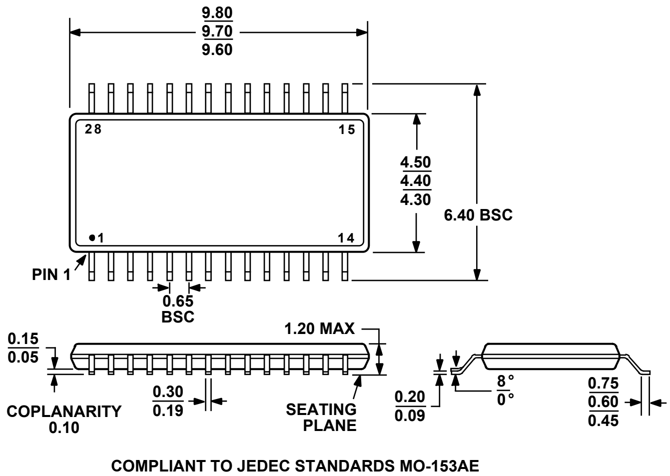

Figure 26. 28-Lead Thin Shrink Small Outline Package [TSSOP]
RU-28
Dimensions shown in millimeters

ORDERING GUIDE

Model	RES (Bit)	DNL (LSB)	INL (LSB)	Temperature Range (°C)	Ordering Quantity	Package Description	Package Option
AD5546BRU	16	±1	±2	–40 to +125	50	TSSOP-28	RU-28
AD5546BRU-REEL7	16	±1	±2	–40 to +125	1000	TSSOP-28	RU-28
AD5556CRU	14	±1	±1	–40 to +125	50	TSSOP-28	RU-28
AD5556CRU-REEL7	14	±1	±1	–40 to +125	1000	TSSOP-28	RU-28

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