OKI Electronic Components

This version: Nov. 2001

KGA4217L

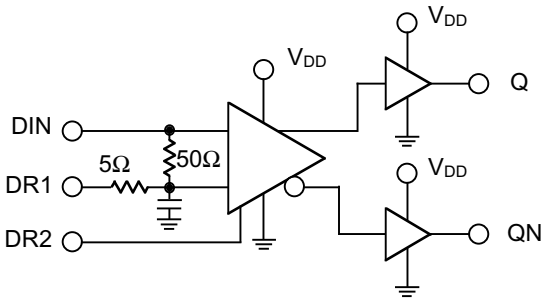
Preliminary

Limiting Amplifier IC

DESCRIPTION

KGA4217L, limiting Amplifier IC with 0.18 µm gate length GaAs MESFETs, has been designed for 10 Gb/s digital communication systems. By using DCFL(Direct Coupled FET Logic), high speed operation of 10 Gb/s and low power dissipation have been realized. Capacitive coupling is recommended for I/O connections.

FUNCTION DIAGRAM



DIN: Data Input
DR1: RF Bypass for data threshold stability
DR2: Data Threshold Control (Duty Cycle Control)
Q, QN: Complimentary Data Outputs
V_{DD}: Power Supply

ABSOLUTE MAXIMUM RATINGS

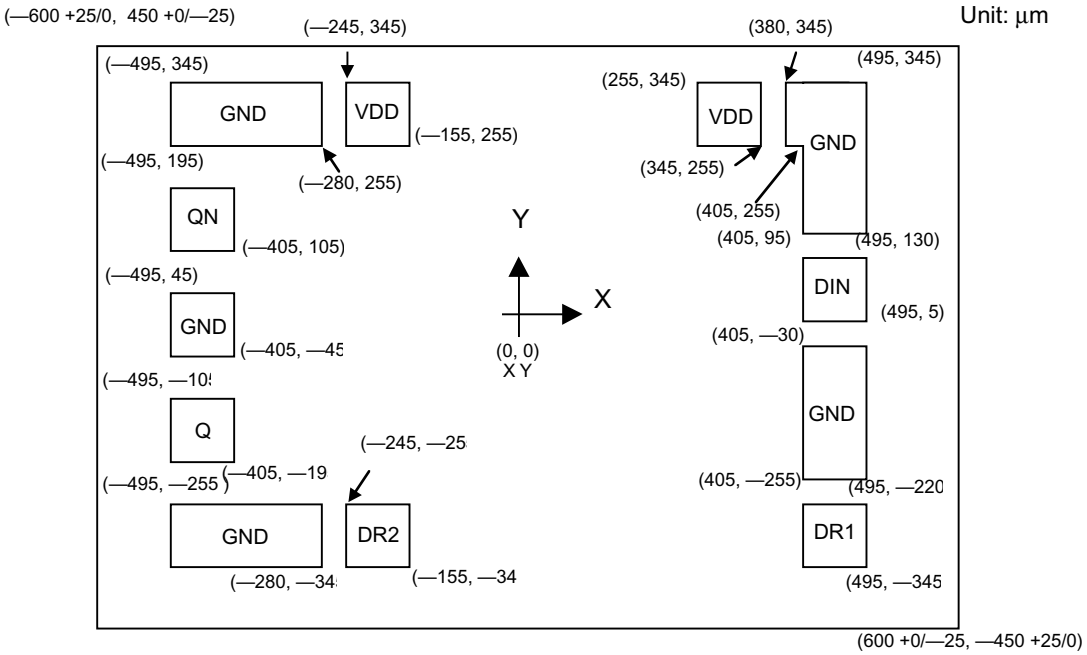
Items	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	—0.3	2.3	V
Applied Voltage at DIN, DR1	VDI	—0.3	1.5	V
Applied Voltage at DR2	VRI	–2.5	2.5	V
Temperature at Package Base under Bias	Ts	—45	100	¡C
Storage Temperature	Tst	—45	125	¡C

ELECTRICAL CHARACTERISTICS

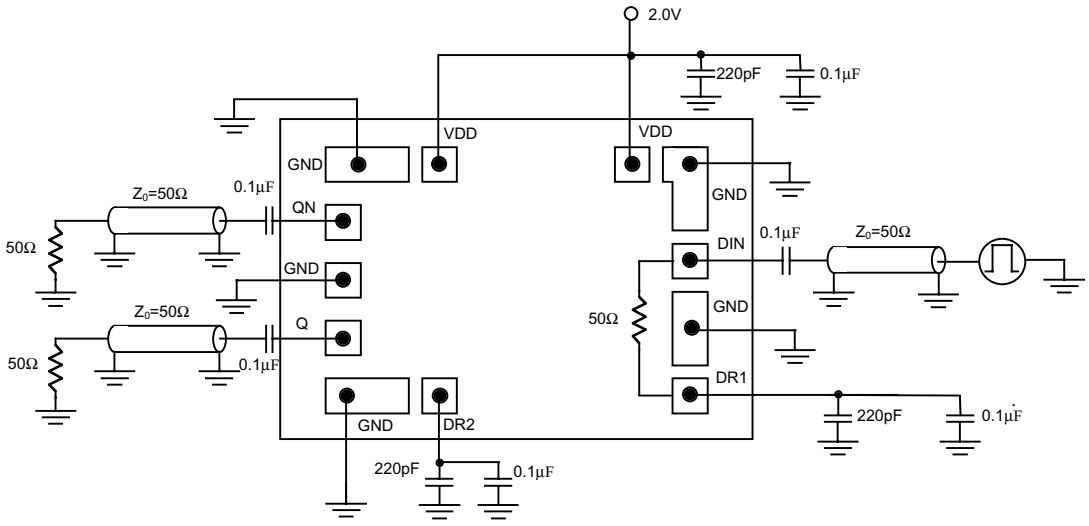
V_{DD} = 2 V ±0.1 V, Ts = 0 to 70°C

Items	Symbol	Min.	Typ.	Max.	Units
Maximum Operating Data Bit Rate	DAR	10			Gb/s
Power Dissipation	PW		0.25	0.35	W
Data Input Voltage Swing	VI	0.035		0.6	Vpp
Data Output Voltage Swing	VO	0.4	0.6	0.9	Vpp

PAD LAYOUT



CONNECTION EXAMPLE

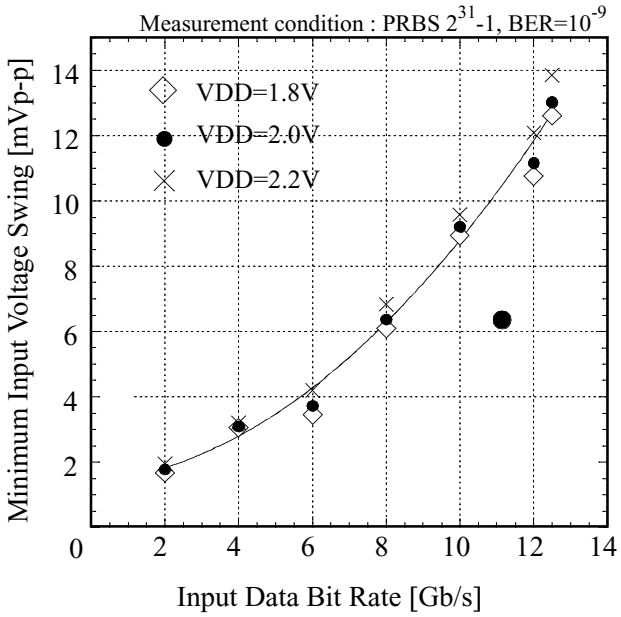


NOTE

- Capacitive coupling is recommended for high speed I/O terminals (DIN, Q, QN).
- DR1 is RF bypass terminal for data threshold level stability and should be connected to ground through RF bypass capacitors (220pF and 0.1 μF). The data threshold level is fixed by

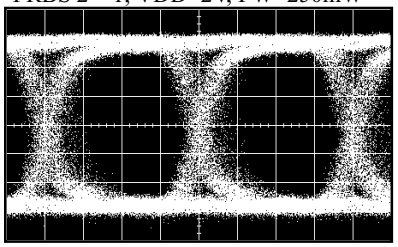
TYPICAL CHARACTERISTICS

Sensitivity vs. Data Bit Rate

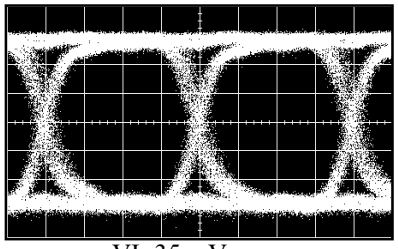


Output Waveforms

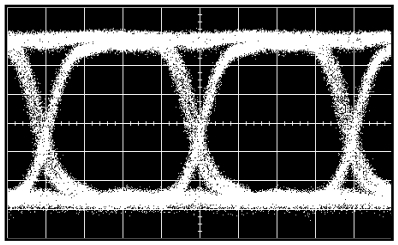
Measurement condition : DAR=10Gb/s, PRBS 2^{31}-1, VDD=2V, PW=250mW



VI=10 mVp-p



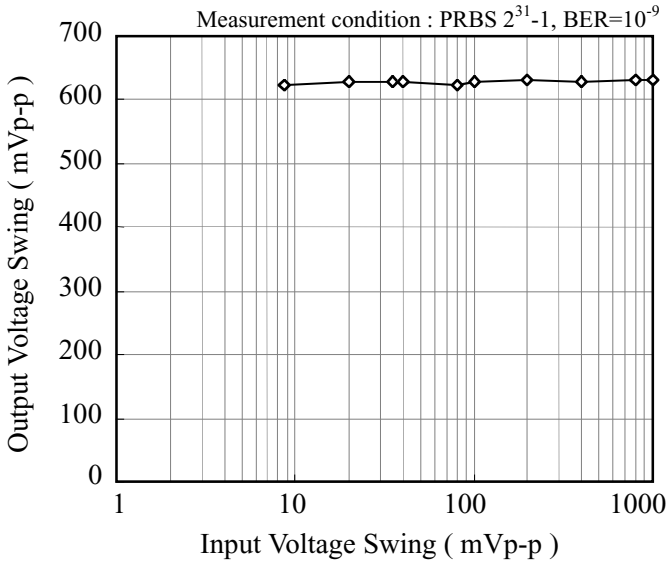
VI=35 mVp-p



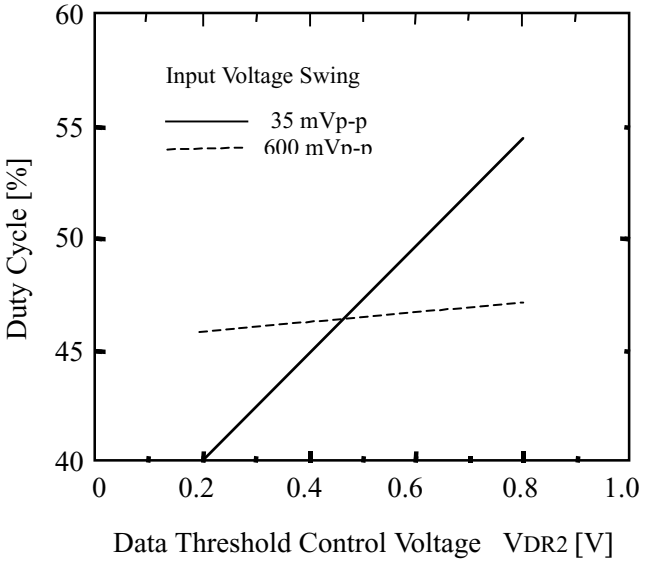
VI=600 mVp-p

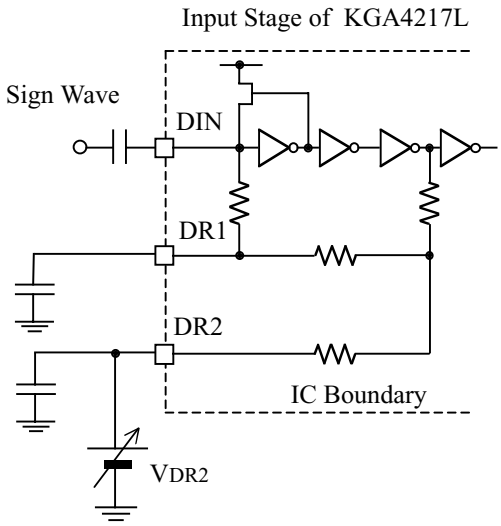
Vert.: 120 mV/div, Horiz.: 25 ps/div

Output Voltage Swing vs. Input Voltage Swing



Duty Cycle vs. Data Threshold Control





EXAMPLE OF DIE MOUNTING