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WT65F4

USB uC with 8KB ISP Flash Memory

12-bit A/D Converter

Data Sheet

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The information in this document is subject to change without notice.

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Table of Content

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Index of Figures

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Index of Tables

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1. General Description

The WT65F4 is single chip Micro-controller with low speed Universal Serial Bus (USB) and A/D functions. It includes an 8-bit 8051 CPU core, 256 bytes SRAM, 8K Bytes Flash memories, 4K boot/ICE ROM, and 32 Programmable I/O. Build-in USB and ND function suitable for UPS, touch pad, joystick & digital board application.

2. Features

- 8051 CPU core
- Internal Oscillator circuit for crystal from 0.5MHz, 1MHz, 2MHz, 4MHz, 6MHz, 8MHz to 12MHz
- 256 bytes SRAM
- 4K byte Internal ROM for ISP and software ICE function use
- 8K bytes Flash Memory
- 4 flash programming modes: parallel, 2-wire ISP, ICE, and normal mode (USB download and RS232 download).
- 32 programmable I/O pins
- 8-pin key wake up function
- Full duplex serial bus for synchronous or asynchronous
- Embedded USB function with three endpoints (one control Enpoint0, two Interrupt IN endpoint)
- Watchdog timer (222 clock cycles time)
- Two 16-bit programmable timers
- Two-channel 8-bit programmable PWM
- ADPCM push-pull DA
- Seven-channel 12-bits rail-to-rail ND converters
- Low VDD reset at 3.5V - 3.7V
- Power on reset
- Support power down/idle power management
- Integrated 3.3V power regulator for USB use
- CMOS technology for Iow power consumption
- Total 4 ports with 25mA Source Current and 8 ports with 25mA Sink Current
- DIP-40, LQFP-48, SDIP-28 or SOP-28 package

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3.Package information

Table 1.WT65F4 Package Types

Package Type	Part Number
LQFP 48	WT65F4-Q48
DIP 28	WT65F4-N28
DIP 40	WT65F4-N40
SOP 28	WT65F4-S28

4.Pin Assignment and Description

Table 2. Pin Descriptions

Pin No.			Pin Name	I/O	Description
48	40	28			
46	1		P1.0	I/O	General purpose I/O with pull-up resister
47	2		P1.1	I/O	General purpose I/O with pull-up resister
48	3		P1.2	I/O	General purpose I/O with pull-up resister
1	4		P1.3	I/O	General purpose I/O with pull-up resister
2	5		P1.4	I/O	General purpose I/O with pull-up resister
3	6		P1.5	I/O	General purpose I/O with pull-up resister
4	7		P1.6	I/O	General purpose I/O with pull-up resister
5	8		P1.7	I/O	General purpose I/O with pull-up resister
6	9	25	RESET	I	Active High external Reset input
7	10	26	P30/RXD	I/O	General purpose I/O with pull-up resister/serial bus receive port
8	11	27	P31/TXD	I/O	General purpose I/O with pull-up resister/serial bus transmit port
9	12	28	P32/INT0	I/O	General purpose I/O with pull-up resister/external interrupt 0
10	13	1	P33/INT1	I/O	General purpose I/O with pull-up resister/external interrupt 1
11	14	2	P34/T0	I/O	General purpose I/O with pull-up resister/Timer 0 external input
12	15	3	P35/T1	I/O	General purpose I/O with pull-up resister/Timer 1 external input
13	16	4	P36/PWM0	I/O	General purpose I/O with pull-up resister/PWM0 output

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14	17	5	P37/PWM1	I/O	General purpose I/O with pull-up resister/PWM1 output
15			VSS	I	Power Ground for DAC
16			DAOUT0	O	DAC output 0
17			DAOUT1	O	DAC output 1
18			VDD	I	Power Source for DAC
19	18	6	XTAL2	O	Oscillator output
20	19	7	XTAL1	I	Oscillator input
21	20	8	VSS	P	Power ground

22	21	9	P20/AD0	I/O	General Purpose I/O with pull-up resistor/ADC channel 0 (25mA Source/Sink current)
23	22	10	P21/AD1	I/O	General Purpose I/O with pull-up resistor/ADC channel 1 (25mA Source/Sink current)
24	23	11	P22/AD2	I/O	General Purpose I/O with pull-up resistor/ADC channel 2 (25mA Source/Sink current)
25	24	12	P23/AD3	I/O	General Purpose I/O with pull-up resistor/ADC channel 3 (25mA Source/Sink current)
26	25	13	P24/AD4	I/O	General Purpose I/O with pull-up resistor/ADC channel 4 (25mA Source/Sink current)
27	26	14	P25/AD5	I/O	General Purpose I/O with pull-up resistor/ADC channel 5 (25mA Source/Sink current)
28	27	15	P26/AD6	I/O	General Purpose I/O with pull-up resistor/ADC channel 6 (25mA Source/Sink current)
29	28	16	P27/Advref	I/O	General Purpose I/O with pull-up resistor/ADC reference voltage (25mA Source/Sink current)
30	29	17	DM	I/O	USB D-signal
31	30	18	DP	I/O	USB D + signal
32	31	19	V33	P	3.3V power regulation output
33	32		P07/K17	I/O	General Purpose IO with pull-up resistor/key interrupt
34	33		P06/K16	I/O	General Purpose IO with pull-up resistor/key interrupt
35	34		PO5/K15	I/O	General Purpose IO with pull-up resistor/key interrupt
36	35		P04/K14	I/O	General Purpose IO with pull-up resistor/key interrupt
37			ICE_N	I	ICE mode input with internal pull-up. Active low.
38			ICESTOP_N	I	Run interrupt in ICE mode with pull-up resistor. Active low
39			P41	I/O	General Purpose IO with pull-up resistor.
40			P40	I/O	General Purpose IO with pull-up resistor.
41	36	20	P03/K13	I/O	General Purpose IO with pull-up resistor/key interrupt
42	37	21	P02/K12	I/O	General Purpose IO with pull-up resistor/key interrupt

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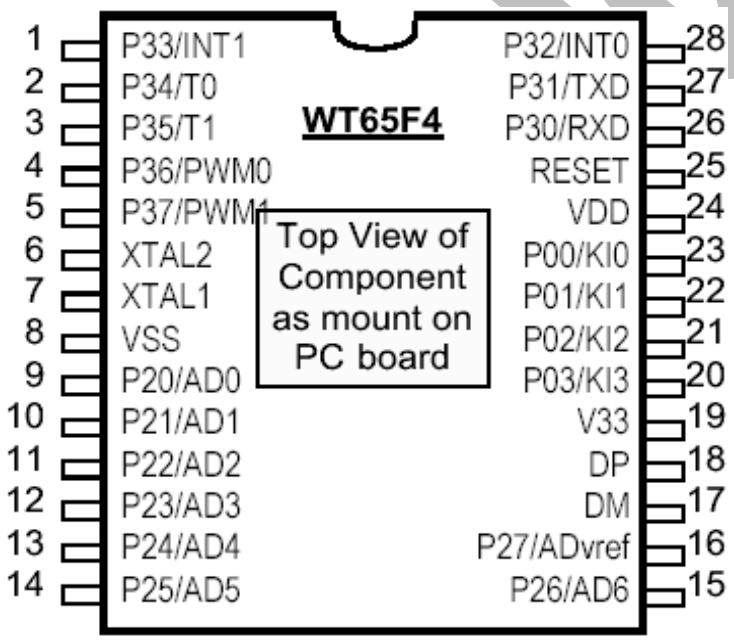
43	38	22	P01/K11	I/O	General Purpose IO with pull-up resistor/key interrupt
44	39	23	P00/K10	I/O	General Purpose IO with pull-up resistor/key interrupt
45	40	24	VDD	I	+5V power supply.

4.1 Pin Configuration



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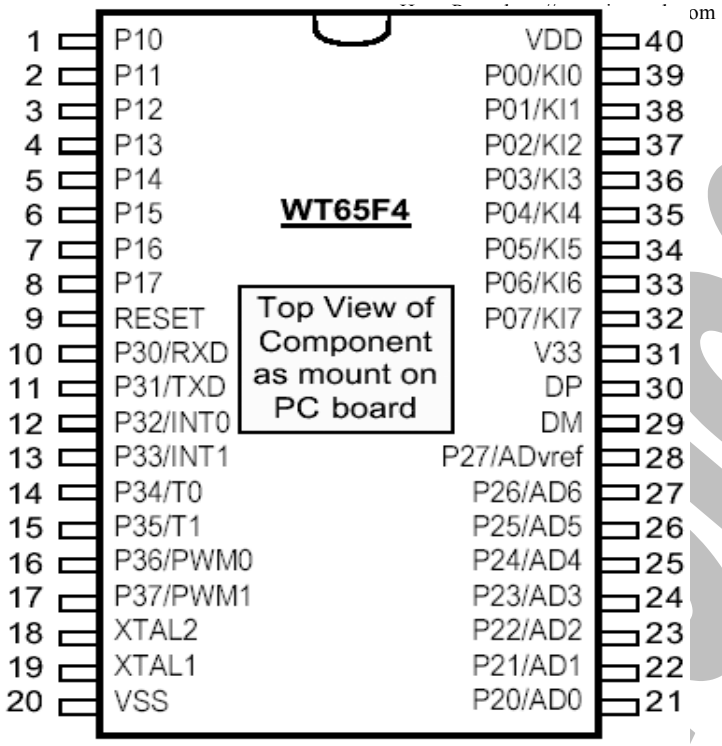

Figure 1. WT65F4 40-pin DIP & 28-pin SOP/DIP package

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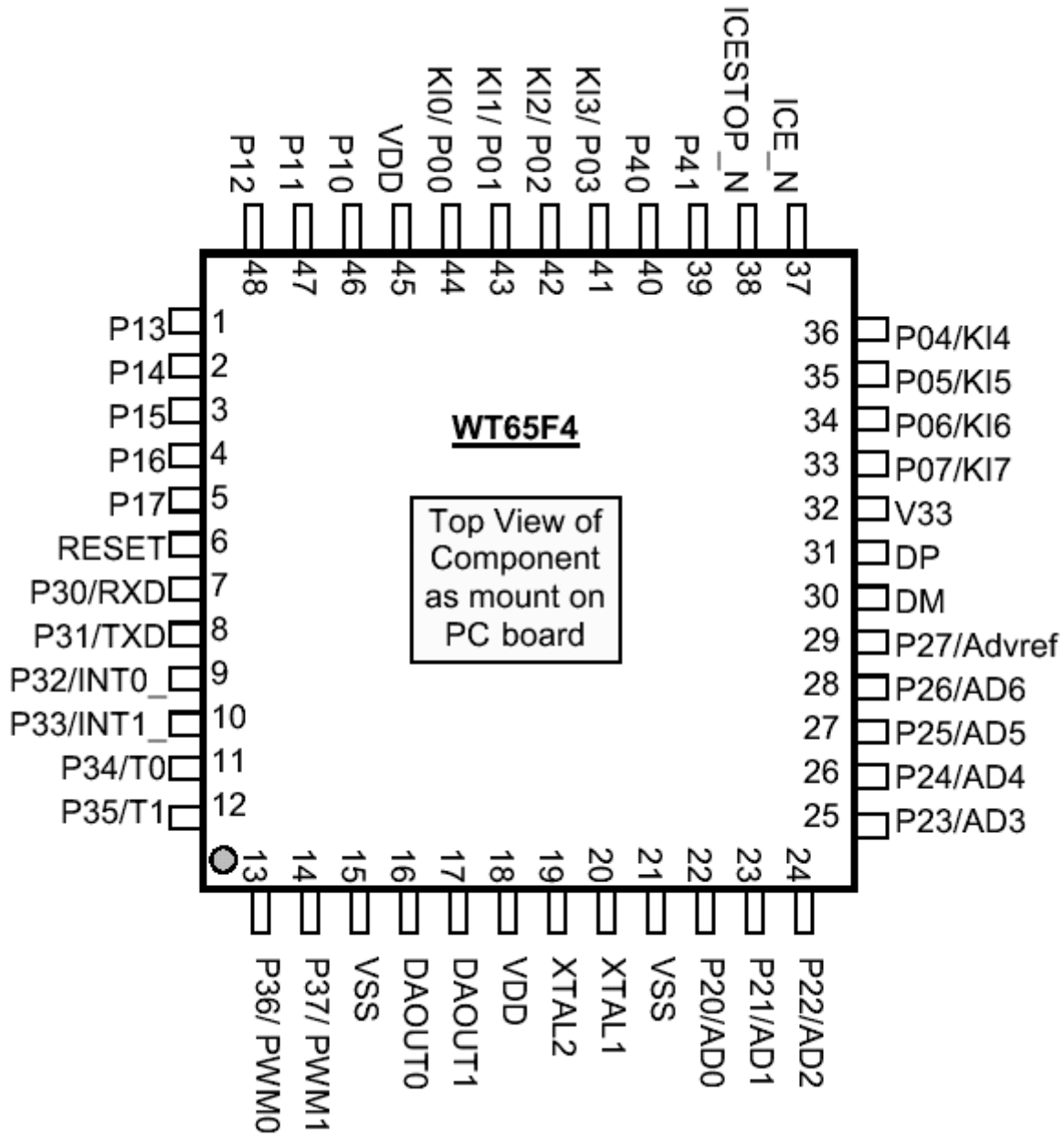

Figure 2. WT65F4 48-pin QFP package

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5.Function Description

The WT65F4 is highly integrated Micro controller with Universal Bus (USB) interface. It contains an 8051 based CPU core, 8K bytes Flash memory, 256 bytes RAM,4K bytes boot / ICE ROM for 2-wire ISP and software ICE function , USB transceiver , Serial bus Interface Engine (SIE), System Interface Logic (SIL) and transmit / receive FIFOs. The USB function supports low-speed data rate (1.5M bps), suspend / resume mode, control / interrupt / bulk transfer and is fully compliant with the USB specification version 1.1.

Operations of the USB interface and special function are controlled through the use of external function registers (XFRs), special function registers (SFRs), SIE, SIL, FIFOs and 8051 microcontroller that are described in the following sections. Figure 3 shows the main functional blocks of the WT65F4 USB module and how they interface with the 8051 CPU.

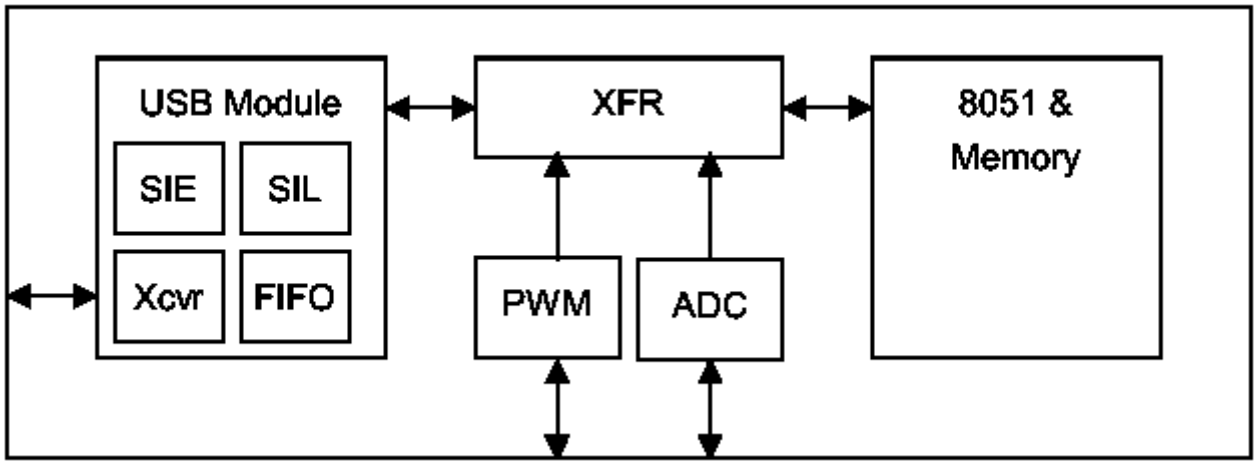

Figure 3.WT65F4 General Block Diagram

5.1 WT65F4 USB Module

The USB function interface manages communications between the Host PC and the USB function. The WT65F4 interface consists of the USB low-speed transceiver, the serial bus engine (SIE), the system interface logic (SIL), and the transmit and receive FIFOs. The USB low-speed transceiver provides the WT65F4 a physical interface to USB lines, the SIE handles communication protocol of USB, and the SIL

handles data transfers and provides the interface among the SIE, the 8051 CPU, the function FIFOs and

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the matrix keyboard.

As shown in Figure 3, the main blocks in the USB module are:

1. **Low Speed USB Transceiver:** This block is an on-chip transceiver having one differential driver to
   transmit the USB data onto the USB bus and single ended receivers on the D+ and D- lines as well as a differential receiver to receive the USB data signal on the USB bus.

2. **Low / Full Serial Bus Interface Engine (SIE):** The SIE does all the front end functions of USB
   protocol such as clock/data separation, syncfield identification, NRZI-NRZ conversion, token packet decoding, bit stripping, bit stuffing, NRZ-NRZI conversion, CRC5 checking and CRC16 generation and checking. Besides, it manages detecting of reset, suspend and resume signals on the upstream port of the WT65F4 to wakeup the system from the suspend state. It also provides serial-to-parallel conversion for the serial packet from the Low Speed USB Transceiver to 8 bit parallel data to the System Interface Logic and
   for 8 bit parallel data from the System Interface Logic to serial packet to the Low Speed USB Transceiver.

3. **System Interface Logic (SIL):** The SIL operates in conjunction with the 8051 CPU to provide the capabilities of controlling the operation of the FIFOs, monitoring the status of the data transactions, transferring event control to the 8051 CPU through interrupt requests at the appropriate moment, initiating resume signaling to USB bus while the WT65F4 is in powerdown mode. Operation of the SIL is controlled through the use of external function registers.

4. **USB Function FIFOs:** The WT65F4 function interface has three endpoints can support serveral types of USB data transfer: control, interrupt and bulk. Endpoint 0 contains one FIFO for transmit and receive, endpoint 1 and endpoint 2 have only one transmit FIFO. Transmit FIFOs are written by 8051 CPU, then read by SIL for transmission. Receive FIFO is written by the SIL following reception, then read by the 8051 CPU. Endpoint 0 supports control transfer for configuration / command / status type communication flows between client software and function. Endpoint 1 and endpoint 2 supports interrupt transfer.

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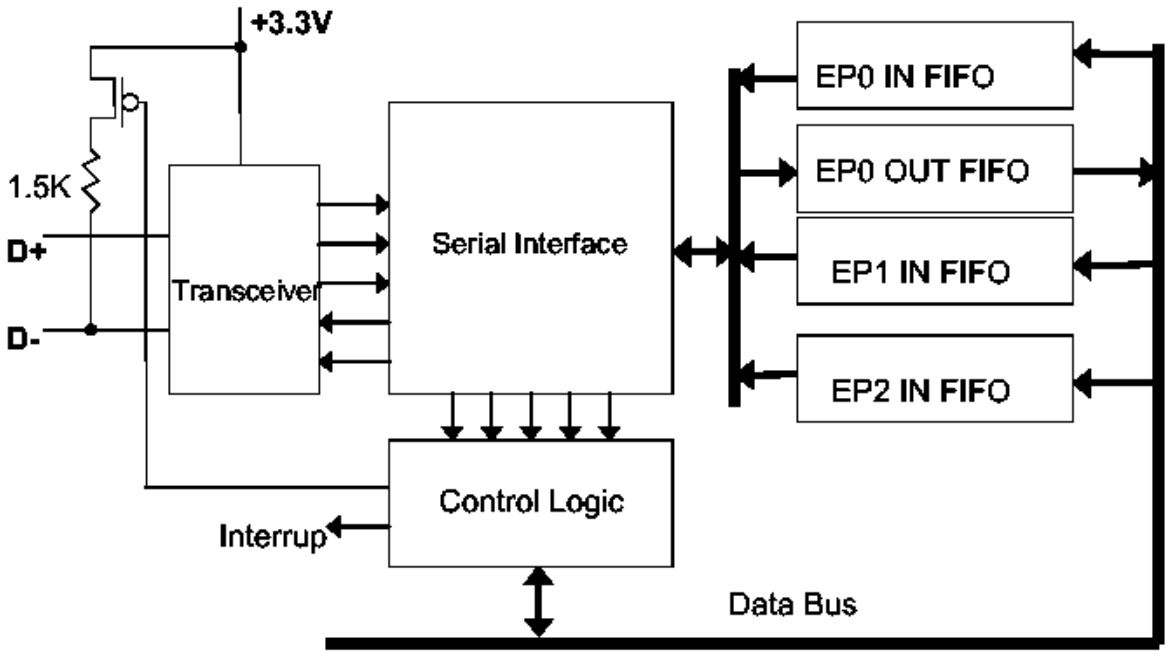

Figure 4. USB Interface Block Diagram

5.2 Microcontroller

The 8051 CPU is a high performance 8 bit on-chip microcontroller running the firmware associated with the operation of the function. It features a 8K-byte FLASH memory, a 256-byte RAM, a 4K-byte boot/ICE ROM, and two 16-bit timers. In addition, the 8051 has two power saving modes enabling further power reduction.

The 8051 CPU's operation speed is the same as the external clock frequency. The main blocks of the 8051 CPU are:

1. **Port 0:** Port 0 is an 8-bit bi-directional I/O port with internal pull-up. Port 0 is assigned as input after reset (i.e., POOE = 00H). The input or output control is depend on the value of SFR POOE. When Port 0 is assigned as output, internal pull-up resistor must be disabled automatically. On the other

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hand, when Port 0
is assigned as input, internal pull-up resistor can be disabled by setting bit 0 of register PUPCTL. Port 0 is also the multiplexed key interrupt and wake-up function during input status.

2. **Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-up. Port 1 is assigned as input after reset (i.e., P1OE = 00H). The input or output control is depend on the value of SFR P1OE. When Port 1 is assigned as output, internal pull-up resister must be disabled automatically. On the other hand, when Port 1
is assigned as input, internal pull-up resistor can be disabled by setting bit 1 of register PUPCTL.

3. **Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-up. Port 2 is assigned as input after reset (i.e., P2OE = 00H). The input or output control is depend on the value of SFR P2OE. When Port 2 is assigned as output or as AD purpose, internal pull-up resister must be disabled automatically. On the other
hand, when Port 2 is assigned as input, internal pull-up resistor can be disabled by setting bit 2 of register PUPCTL. Port 2 is also the multiplexed analog to digital converter (ADC) function during high-impedance inputs. To be an I/O port, the enhanced internal circuits can directly drive outside components such as LED, buzzer, etc. All of the ports can offer source and sink currents about 25mA.

4. **Port 3:** Port 3 is an 8-bit bi-directional I/O port with internal pull-up. Port 3 is assigned as input after reset (i.e., P3OE -- 00H). The input or output control is depend on the value of SFR P3OE. When Port 3 is assigned as output, internal pull-up resister must be disabled automatically. On the other hand, when Port 3
is assigned as input, internal pull-up resistor can be disabled by setting bit 3 of register PUPCTL. Port 3 also serves the functions of various special features as listed below:

Port Pin	Alternate Function
P30	RXD(serial input port)
P31	TXD(serial output port)
P32	INT0(external interrupt 0)
P33	INT1(external interrupt 1)
P34	T0 (timer 0 external input)
P35	T1 (timer 1 external input)
P36	PWM0 (PWM 0 output port)
P37	PWM1 (PWM 1 output port)

5. **Port 4:** Port 4 is an 2-bit bi-directional I/O port with internal pull-up. Port 4 is assigned as input

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after reset (i.e., P4OE = 00H). The input or output control is depend on the value of SFR P4OE. When Port 4 is assigned as output, internal pull-up resister must be disabled automatically. On the other hand, when Port 4 is assigned as input, internal pull-up resistor can be disabled by setting bit 4 of register PUPCTL.

6. **16-bit Timer:** The WT65F4 has two 16 bits timers that can be clocked by Oscillator. It can be programmed for applications such as periodically generating interrupt or serving as a firmware watchdog timer etc.

7. **8051 On-Chip Memory:** The 8051 provides on-chip program memory beginning at location 4000H in normal mode, testing mode, and parallel programming mode. where, following chip reset, the first instruction is fetched and executed Flash memory. The 8051 CPU also provides on-chip data RAM beginning at location 00H. Locations 00H-7FH can be accessed with direct, indirect addressing while locations 80H-FFH can only be accessed with indirect addressing. In 2-wire ISP programming mode and ICE mode, the program memory begins at location 4000H. In ICE mode, the address is continuesly compared with both BRK0 and BRK1 SFR registers. If a match occurs, a breakpoint interrupt (i.e., NMI)is issured and the address is jumped to $8010h.

ROM Type	Memory Location
Flash ROM 8K Byte	000h-1FFFh
Boot boot/ICE ROM 4K Byte	8000h-8FFFh

Figure 5. Memory mapping of Flash ROM, boot ROM, and ICE ROM

The following flash addresses are reserved for special purpose:

$0000h : program-reset vector.
$0003h : external interrupt 0, Key scan input or A/D interrupt vector.
$000Bh : timer 0 interrupt.
$0013h : external interrupt 1 or USB interrupt vector.
$001Bh : timer 1 interrupt.
$0023h : serial bus interrupts.
$8010h : breakpoint interrupt for ICE mode

5.3 Analog to Digital Converter (ADC)

The seven channels of 12-bits AD converter is turned on by ADON bit (Table 31). ADSEL0, 1, and 2 are the channel selected bits to control which channels' signal will be converted. The input analog signal will be converted to digital and stored in register ADH and ADL. As the ADINT_IE (Table 14) being set to

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"1" after AD be converted , interrupt occurs and ADINT (Table 13) is set to "1",AD block show in Figure 6.

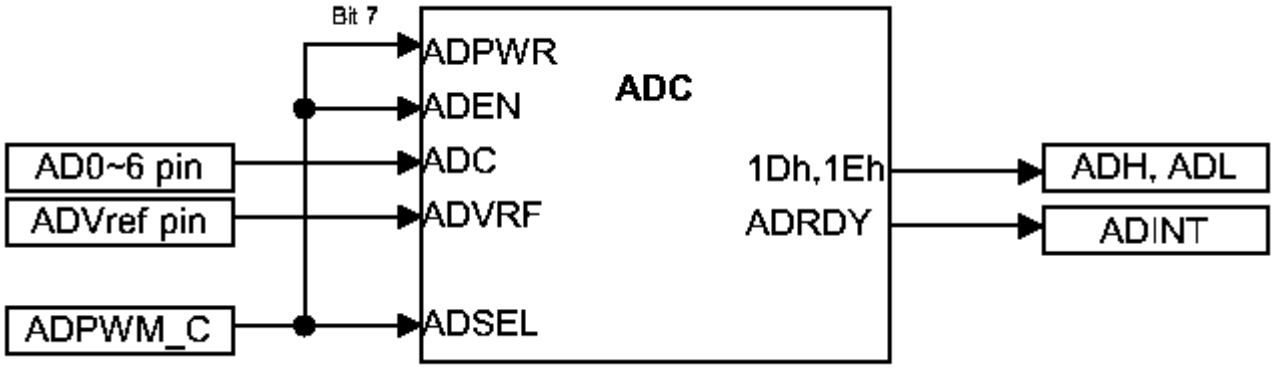

Figure 6.ADC Interface Diagram

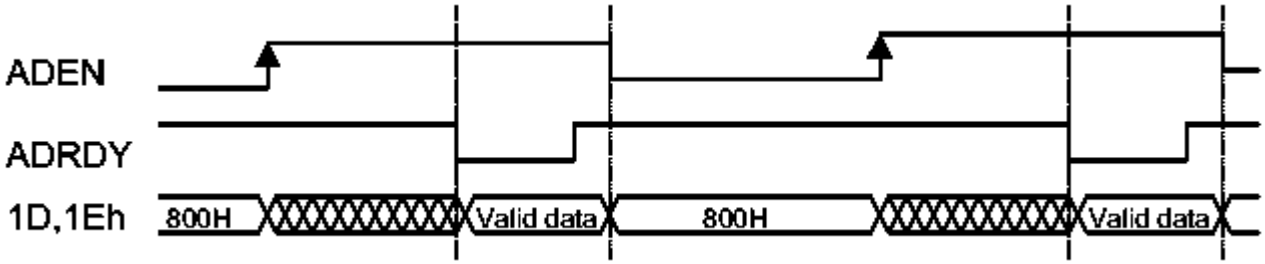

Figure 7. ADC Timing Diagram

Table 3. ADC Interface Description

Signals	I/O	Description
DAON	I	0:Power-down mode;1:ADC turned on
ADEN	I	Conversion start. Rising edge trigger
AD0~6	I	AD analog inputs
ADVRF	I	AD reference voltage.1uF capacitor must be connected between ADVRF and VSS
CLKIN	I	ADC clock input
1DH,1EH	O	AD digital output bus. Q is available from ADRDY rising edge to ADEN becoming low.
ADRDY	O	AD output ready. Rising edge triggered

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5.4 Pulse Width Modulation (PWM)

The corresponding PWM register (Table 24 and Table 25) controls the PWM duty cycle. Duty cycle ranges from 0/32 to 31/32. The LSB 3-bit of the PWM register determines the frame to be extended two Tosc (Tosc = 1/external clock frequency).

000 : no extended pulse.
001 : extended two Tosc at frame 4.
010 : extended two Tosc at frame 2 and 6.
011 : extended two Tosc at frame 2, 4 and 6.
100 : extended two Tosc at frame 1, 3, 5 and 7.
101 : extended two Tosc at frame 1, 3, 4, 5 and 7.
110 : extended two Tosc at frame 1,2, 3, 5, 6 and 7.
111 : extended two Tosc at frame 1, 2, 3, 4, 5, 6 and 7.

The MSB 5-bit of PWM register determines 0/32 to 31/32 duty cycle in each frame. However, both PWM0 and PWM1 duty cycles can be extended depending on the value of ADPWMCLK register. This can be done by dividing the external clock to the desired frequency (new Tosc), and then generate the pulse width according to the MSB 5-bit of PWM register. Figure 8 shows three examples of how PWM pulses are extended.

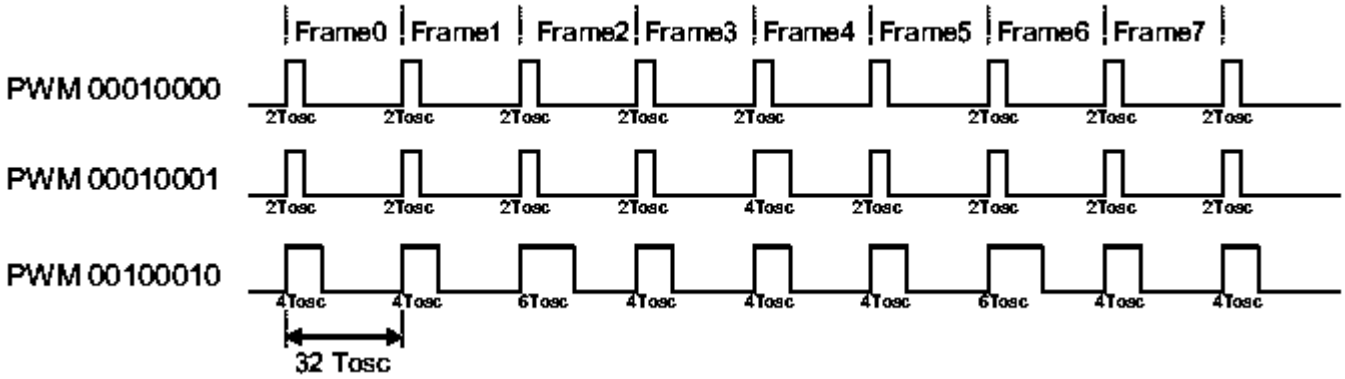

Figure 8. PWM Output Waveform Diagram

5.5 ADPCM push-pull DIA

Two voice envelope register buffers, SPKENV0 and SPKENV1, are added in XFR. If ADPCM is enabled (i.e., setting SPKON bit to high), P36/PWM0 and P37/PWM1 outputs the value from ADPCM push-pull DA. Otherwise, PWM output are selected. The bit DUALT indicates whether two envolope datas needs to be combined together in order to generate the dual tone.

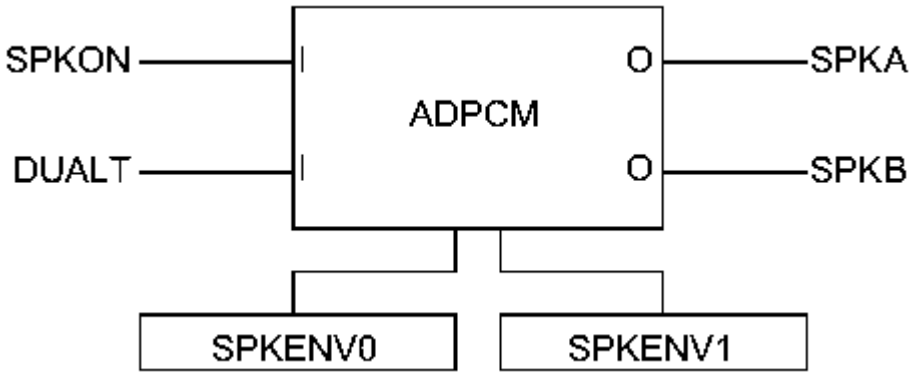

Figure 9. ADPCM block diagram

5.6 WT65F4 Address Space Mapping

The WT65F4 has five address spaces: a program memory space, an internal data memory space, a special function register space, an external function register space, and a register file. Table 4 shows the addressing mapping if the WT65F4.

Table 4. Addressing mapping

Memory Type	Size	Location	Data Addressing
Flash Code	8K bytes	0000H-1FFFH	Indirect using MOVC instruction
External Function Register	32 bytes	00H-1FH	Indirect using MOVX instruction
Internal Data	128 bytes	00H-7FH	Direct, Indirect
	128 bytes	80H-FFH	Indirect
SFRs	128 bytes	80H-FFH	Direct
Register File	8 bytes	R0-R7	Register

Note : Direct : Direct Byte Addressing

Indirect: Indirect Byte Addressing

(1) : Please refer to 8051 data sheet for bit definition of each SFR.

5.7 WT65F4 Special Function Register Address Space

The special function registers (SFRs) reside in this optimized 8051 microcontroller Core. Table 5

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lists the location of all the WT65F4 SFRs. Please refer to the 8051 Data sheet for bit definition of each SFR.

Table 5. WT65F4 Special Function Register (SFR) layout

Name	Address	R/W	initial	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	80h	RW	FFh	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h	RW	07h								
DPL	82h	W	00h								
DPH	83h	W	00h								
P0OE	84h	W	00h	P07OE	P06OE	P05OE	P04OE	P03OE	P02OE	P01OE	P00OE
PCON	87h	RW	0x010000b	SMOD	--	ISPM	ICE(1)	GF1	GF0	PD	IDL
TCON	88h	RW	00h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMODE	89h	RW	00h	GATE	C/T	M1	M0	GATE	C/T	M1	MO
TL0	8Ah	RW	00h	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00
TH0	8Ch	RW	00h	TH	TH	TH	TH	TH	TH	TH	TH

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	h			07	06	05	04	03	02	01	00
TL1	8Ch	RW	00h	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10
TH1	8Dh	RW	00h	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10
P1	90h	RW	FFh	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P1OE	94h	W	00h	P17OE	P16OE	P15OE	P14OE	P13OE	P12OE	P11OE	P10OE
SM2	98h	RW	00h	SM0	SM1	SM3	REN	TB8	RB8	TI	TI
SBUF	99h	RW	XXh	S7	S6	S5	S4	S3	S2	S1	S0
P2	A0h	RW	FFh	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P2OE	A4h	W	00h	P27OE	P26OE	P25OE	P24OE	P23OE	P22OE	P21OE	P20OE
IE0	A8h	RW	0xx00000b	EA	--	--	ES	ET1	EX1	ET0	EX0
P3	B0h	RW	FFh	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P3OE	B4h	W	00h	P37OE	P36OE	P35OE	P34OE	P33OE	P32OE	P31OE	P30OE
IP	B	R	xxxx	--	--	--	P	P	P	P	P

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0	8h	W	xx00b				S	T1	X1	T0	X0
PSW	D0h	RW	00h	CY	AC	F0	RS1	RS0	OV	--	P
P4(2)	E8h	RW	xxxxxx00b	--	--	--	--	--	--	P41	P40
P4OE	C8h	W	xxxxxx00b	--	--	--	--	--	--	P41OE	P40OE
ACC	E0h	RW	00h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0h	RW	00h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
PCSK0	E6h	R	00h	PCC7	PCC6	PCC5	PCC4	PCC3	PCC2	PCC1	PCC0
PCSK1	E7h	R	00h	PCC15	PCC14	PCC13	PCC12	PCC11	PCC10	PCC9	PCC8
PUPCTL	E9h	W	00h	--	--	--	P4PUP	P3PUP	P2PUP	P1PUP	P0PUP
BRKEN	EAh	W	00h	--	--	--	--	--	BKEN2	BKEN1	BKEN0
BRK0L	EBh	W	00h	B0.7	B0.6	B0.5	B0.4	B0.3	B0.2	B0.1	B0.0
BRK0H	ECh	W	00h	B0.1	B0.1	B0.1	B0.1	B0.1	B0.10	B0.9	B0.8

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				15	4	3	2	1			
BRK1L	I h	W	00h	B1.7	B1.6	B1.5	B1.4	B1.3	B1.2	B1.1	B1.0
BRK1H	I h	W	00h	B1.15	B1.14	B1.13	B1.12	B1.11	B1.10	B1.9	B1.8

(1) Read only (2) Bit addressable

5.8 External Function Register Address Space

The external function registers (XFRs) reside inside the USB module. The 8051 is connected to one of these registers when the register is addressed by the contents of registers R0 or R1 in the internal data memory. Two instructions, MOVX @Rr, A and MOVX A, @Rr can be used for data movement between the XFRs and accumulator of the 8051. Table 6 lists the location of all the XFRs. When the instruction, MOVX @Rr, A or MOVX A, @Rr, is executed, the address contained in R0 or R1 registers is latched by ALE signal and then the direction of data movement between the XFRs and the 8051 can be controlled by the signals WR or RD subsequently generated by the 8051.

Table 6. External Function Register (XFR) layout

Name			Initial	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FADDR			00h	--	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
USBI			xx0000 00b	--	--	RESUME	SUSPEND	USBx0INT	USBTx2INT	USBTx1INT	USBTx0INT
USBKAIE			00h	KINT_IE	ADINT_IE	RESUME_IE	SUPEND_IE	Rx0INT_IE	Tx2INT_IE	Tx1INT_IE	Tx0INT_IE
SIEI			Xx0000	--	--	LV	CLK12M	V33	USBRSTE	DM	WA

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			0b			REN	EN	EN	N	EN	KEUP
EPINDEX			xxx xxx 00b	--	--	--	--	--	--	EPINX1	EPINX0
EPCON			001 x01 01b 3	RXSTL	TXSTL	CTLEP	--	RXIE	RXEPEN	TXOE	TXEPEN
SPWDCTL			000 000 10h	SPKON	DUALT	--	--	--	--	EN_WDT	WDTRST
TXCAT			xxh	TXDAT7	TXDAT6	TXDAT5	TXDAT4	TXDAT3	TXDAT2	TXDAT1	TXDAT0
TXCON			0xx xxx xxb	TXCLR	--	--	--	--	--	--	--
TXFLG			xxx x10 00b	--	--	--	--	TXEMP	TXFULL	TXURF	TXOVF
TXCNT			00h	--	--	--	--	TXCNT3	TXCNT2	TXCNT1	TXCNT0
TXSTAT			00h	TXSEQ	--	--	--	--	TXVOID	TXERP	TXACK
PWM0			00h	PWM07	PWM06	PWM05	PWM04	PWM03	PWMO2	PWM01	PWM00
PWM1			00h	PWM17	PWM16	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10
P0ODCTL			00h	--	--	P05SN	P04SN	--	--	P01SN	P00SN
SPKENV0			00h	DA0.7	DA0.6	DA0.5	DA0.4	DA0.3	DA0.2	DA0.1	DA0.0
ISPCTL			xxh	XE	YE	SE	OS	ERASE	PROG	MAS1	NVSTR
ISPADDL			xxh	--	--	--	YAD	YAD	YAD	YAD	YAD

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							R4/A4	R3/A3	R2/A2	R1/A1	R0/A0
ISPADDH			xxh	XADR7/A12	XADR6/A11	XADR5/A10	XADR4/A9	XADR3/A8	XADR2/A7	XADR1/A6	XADR0/A5

ISPDATA			xxh	D7	D6	D5	D4	D3	D2	D1	D0
ADPWM_C			xxxxxx10b	ADON	ADEN	ADSLE2	ADSEL1	ADSEL0	Adverf_C	PWMEN1	PWMEN0
ADCLK			000000 00b	--	-	--	--	--	ADCLK2	ADCLK1	ADCLK0
KYADI			00xxxx xxb	KEYINT	ADINT	--	--	--	--	--	--
RXDAT			xxh	RXDAT7	RXDAT6	RXDAT5	RXDAT4	RXDAT3	RXDAT2	RXDAT1	RXDAT0
RXCON			0xxxxx xxb	RXCLR	--	--	RXFFRC	--	--	--	--
RXFLG			xxxx10 00b	--	--	--	--	RXEMP	RXFULL	RXURF	RXOVF
RXCNT			00h	--	--	--	--	RXCNT3	RXCNT2	RXCNT1	RXCNT0
RXSTAT			00h	RXSEQ	RXSETUP	STOVW	EDOVM	--	RXVOID	RXERR	RXACK
ADL			00h	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
ADH			00h	--	--	--	--	AD	ADB1	AD	ADB

								B 11	0	B9	8
SP KE NV 1			00h	D A 1. 7	D A 1. 6	D A 1. 5	D A 1. 4	D A 1. 3	DA 1.2	D A1 .1	D A1 .0

Note : (1) Read to clear

(2)Write 0 to clear

(3) Initial value only for Endpoint 0

5.9 Clock Unit

Several different external clock frequencies can be applied to WT65F4, they are 0.5MHz, 1MHz, 2MHz, 4MHz, 6MHz, 8MHz, and 12MHz. An feedback resistor is built in and can be turned off during power-down mode and be waked up by a key interrupt, an external interrupt, or the resume signal from USB host.

When USB function is used, only 6MHz or 12MHz external clock can be used. As USB core only accepts 6MHz, when 12MHz clock is applied, bit 4 of SIEI register is set so that a divided-by-2 circuit is activated.

There are two different internal clock speed to be applied to WT65F4 USB functions, 1.5MHz and 6MHz. The implementation of the two internal clocks is shown below:

Table 7. Internal clock generation map

	USB low speed	**USB low speed**	**No USB**
External clock	6MHz	12MHz	Spec
%2	Disable	6MHz	Disable
DPLL	1.5MHz	1.5MHz	Disable

Note: %2 means divided-by-2 circuit

DPLL means divided-by-4 digital PLL.

As shown in Figure 10, the clock to CPU control section is stopped where "1" is set in bit 0 (IDL) of the power control register (PCON) in firmware, thereby the CPU operation is halted in idle mode. Idle mode

freezes the clocks to the CPU at known states while the peripherals continue to be clocked. The CPU status before entering idle mode is preserved. The contents of the SFRs, XFRs and RAM are also retained. Idle mode can be used while the device is in unenumerated state following chip reset. Activation of an enabled interrupt and a logic high on chip reset are the ways to exit the idle mode.

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The clock to where the CPU controlled section and peripherals that including some portions of USB function is stopped at where bit 1 (PD) of the power control register (PCON) is set in firmware. Therefore both Oscillator and CPU operation are halted in powerdown mode. The CPU status before entering powerdown mode is preserved. In addition, the contents of the SFRs, XFRs and RAM are also retained. For suspend, firmware must put the WT65F4 into powerdown mode to meet the USB limitation of 500 μA. Activation of an enabled interrupt and a logic high on chip reset are the ways to exit the powerdown mode.

The clock source usb_clock is used as the sampling clock for the USB function for Low (6MHz and 1.5MHz) speed USB Transactions.

Besides of clock generated for USB core logic and 8051 CPU, WT65F4 also needs to generate a clock source for AD Convertor (ad_clk). The speed of ad_clk depends on ADSEL bits in ADPWM_C register. Please see Table 31 for detail.

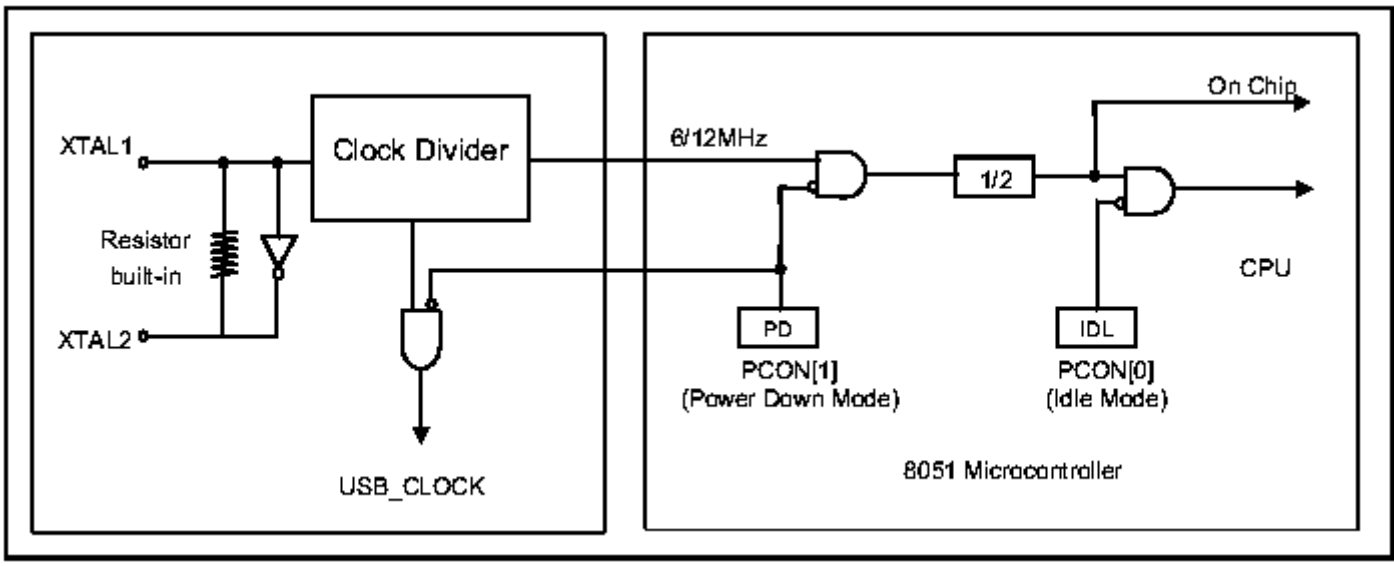

Figure 10. Clock circuit when USB function is used

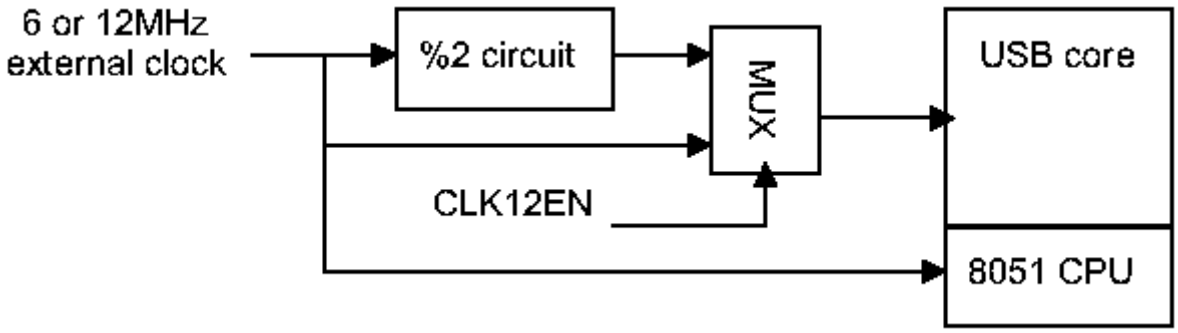

Figure 11. Clock divided-by-2 circuit

5.10 Reset

Chip reset can be initiated by the watch-dog timer reset, or Low voltage reset, an USB-initiated reset, an power-on reset (POR), or an external high level reset. The external reset must be applied to the RESET pin for at least 80ms while the Oscillator is runningin order to reset the entire chip. A Low voltage (VCC V_{LvR}) causes a reset condition for entire chip to prevent the chip Flash memory being placed at unknown state. 8051 reset is extended for 5 states in order to synchronize ALE and PSEN.

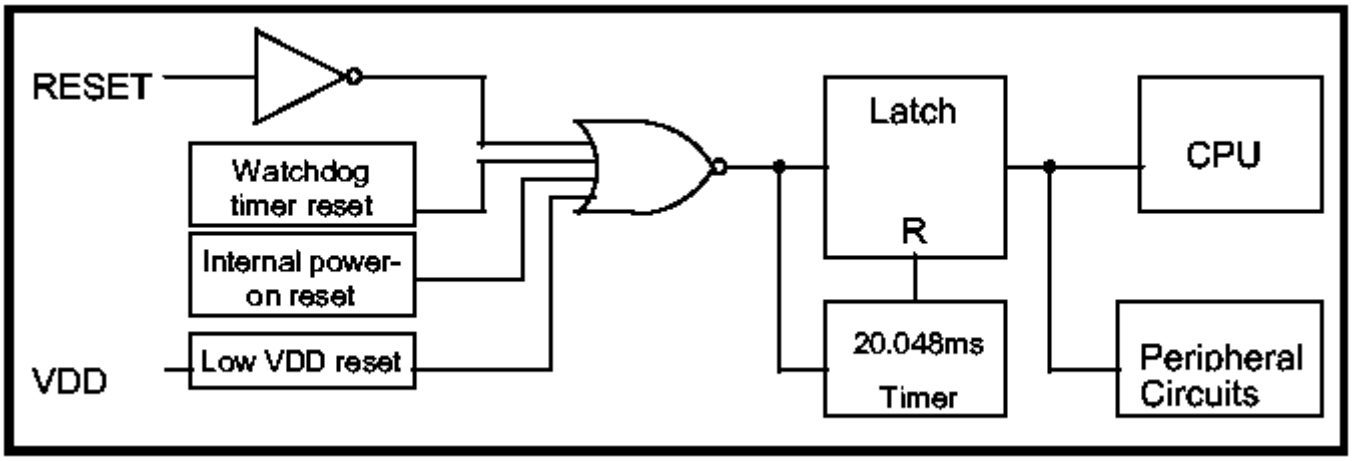

Figure 12. Reset Signals

5.11 Powerdown Mode and Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the idle mode is activated. Once in the idle mode the CPU status is preserved in its entirety. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware and then the idle mode is terminated.

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The instruction that sets PCON.1 is the last executed prior to entering powerdown mode. Once in the powerdown mode, the Oscillator is stopped. The contents of the on-chip RAM, the Special Function Registers and USB External Function Registers are saved. Hardware reset and activation of any enabled interrupt is the ways of exiting the powerdown mode. Powerdown mode should be used for USB suspend
operation. PCON.1 has to be set in the ISR of interrupt caused by active SUSPEND signal. Please see section 5.12 for details.

The WT65F4 can initiate resume signaling to the USB host through remote wakeup of the USB function while it is in powerdown mode. While in powerdown mode, remote wakeup has to be initiated through assertion of an enabled external interrupt.

ADC powerdown mode is controlled by ADPWR bit of ADPWM_C register.

5.12 Interrupt

As shown in Figure 14, there are 6 interrupt sources share two interrupt inputs of the 8051 (interrupt 0 and interrupt 1):

Interrupt 0 This interrupt is connected to the external hardware interrupt input P32/INT0 of the WT65F4.

Two interrupts, AD interrupt (ADINT) and keyboard interrupt (KEYINT), also use interrupt 0
to operate. In normal operation, both AD interrupt and keyboard interrupt is disabled. In powerdown mode, AD interrupt would be disable and keyboard interrupt is enable to terminate
the powerdown mode (suspend state) and support remote wakeup. The interrupt vector is 03H.
The external interrupt P32/INT0 can only be used when both ADINT and KEYINT interrupt
functions are disabled. Figure 13 shows the control block diagram of P32/INT0, ADINT, and
KEYINT.

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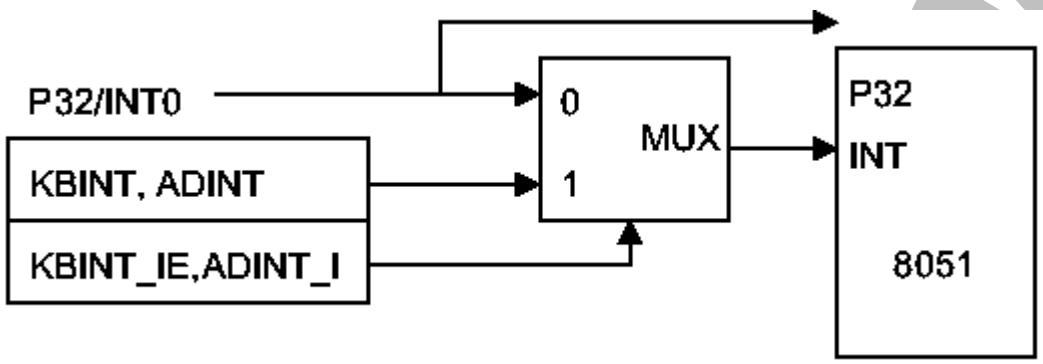

Figure 13. Block Diagram of INT0

Interrupt 1 This interrupt is used by USB function interrupt and connected to the external hardware interrupt input 1 (P33/INT1) of WT65F4. This interrupt is used for control transfer and interrupt transfer and its interrupt vector is 13H. This interrupt is also initiated by assertion of an USB suspend interrupt signal or an USB resume interrupt signal. Similar to interrupt 0, the external interrupt P33/INT1 can not be used when anyone of the USB interrupt functions is enabled.

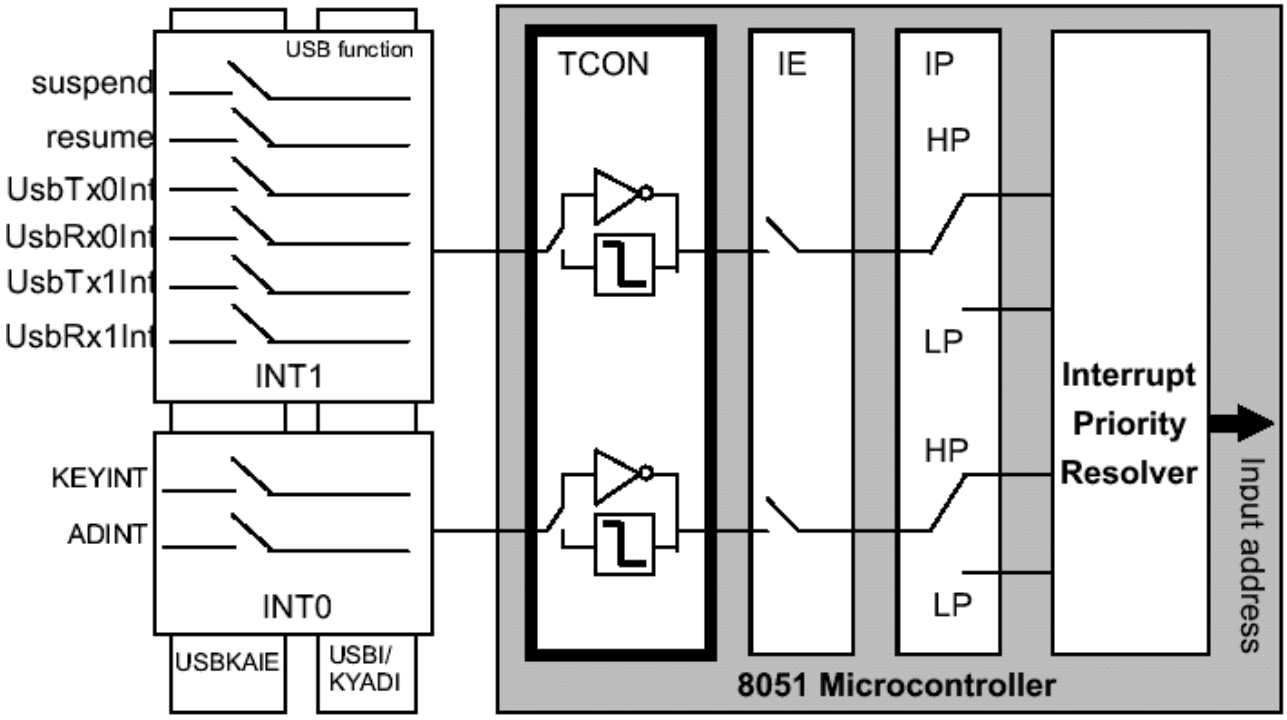

Figure 14. Wt65F4 interrupt circuit

5.13 Function Endpoint

The WT65F4 can supports up to three function endpoints. Endpoint 0 contains a FIFO for transmit and receive while endpoint 1 and endpoint 2 is transmitted only. Endpoint 1 and endpoint 2 handles interrupt data transfer. The EPINDE ~ register (Table 16) selects the endpoint for any given data transaction.

5.14 Transmit FIFOs

The WT65F4 has one transmit FIFO for each function endpoint (See Figure 4).

5.15 Transmit FIFOs Features

The transmit FIFOs are data buffers with the following features (See Figure 15):

- support for one data set of not greater than 8 bytes
- a byte count register to store the number of bytes in the data set
- protection against overwriting data in a full FIFO
- capability to retransmit the current data set

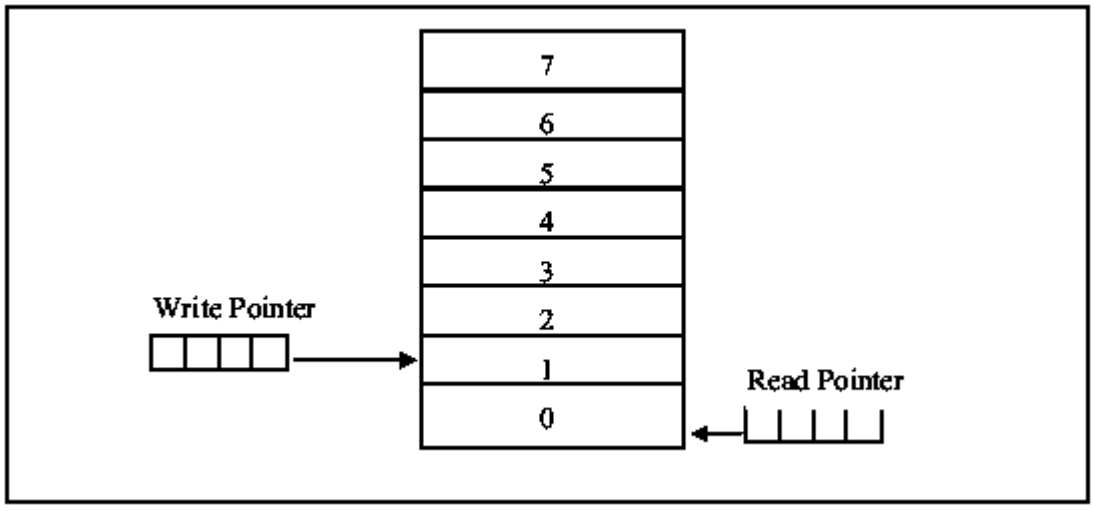

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Figure 15. Transmit FIFO outline

The 8051 CPU writes to the FIFO location specified by the write pointer also used as the byte-counter to
indicate how many bytes have been written and not yet read by SIL. The write pointer automatically increments by one after a write and decrements by one after a read. The read pointer points the next FIFO location to be read by the SIL. The read pointer automatically increments by one after a read. The transmit
FIFO is inhibited to be read by the SIL when it is empty or before a data set has been successfully written into it.

5.16 Transmit Data Set Management

TXFULL = 1 in the TXFLG register (Table 21), indicates data set has been written into the FIFO and is ready for transmission. Following reset, TXFULL -- 0 and TXEMP = 1, signifying an empty FIFO. Only the first eight bytes of the data set which size is greater than eight are written into the FIFO. In this case, TXFULL is not set until a write to TXCNT (Table 22). In the case of TXFULL = 1 farther writing to TXDAT (Table 19) or TXCNT are ignored. Please note that the content of TXCNT determines the number of bytes transmitted over the USB lines. Discrepancy between the byte number written to TXCNT and number of bytes actually written to the FIFO will cause an unexpected result. Read the FIFO is prohibited when the FIFO is empty or TXFULL = 0.

Two events cause the TXFULL to be updated:

- A new data set is written to the FIFO: The CPU writes bytes to the FIFO via TXDAT and writes the number of bytes to TXCNT. TXFULL is only set after the write to TXCNT. Set TXCNT-0 indicates a zero length transmission. In this case, TXFULL is set and TXEMP remains unchanged to indicate the FIFO is still empty. This process is illustrated in Table 8.

- A data set in the FIFO is successfully transmitted: The SIL reads the data set Flashmemory the FIFO for transmission. When a good transmission is acknowledged, the TXFULL is cleared and TXEMP is set.

Table 8. Writing to the Byte Count Register

TXFULL	TXEMP	Zero Length Transmission	Write bytes to TXDATx → → Write byte count to TXCNTx	Data Set Written	TXFULL	TXEMP
0	0	NO		Yes	1	0
0	1	NO		Yes	1	0
0	1	Yes		No	1	1
1	-	-		Write Ignored	1	-

When a good transmission is completed, both read pointer and write pointer is advanced to the start point of the FIFO to set up for transmitting the next data set. When a bad transmission is encountered, the read pointer is reversed to the start point of the FIFO to enable the SIL to re-read the last data set for retransmission. The pointer reversal and advance are accomplished automatically by hardware. Table 13 summarizes how actions following a transmission depend on TXERR and TXACK.

Table 9. Truth table for transmit FIFO management

TXERR	TXACK	Action at End of Transfer Cycle
0	0	No at End of Transfer Cycle
0	1	Read Pointer and Write Pointer both are set to the start point of FIFO
1	0	Read Pointer is set to the start point of FIFO

5.17 Transmit FIFO Registers

TXDAT, the transmit FIFO data register (see Table 19 and Section 0)
TXCNT, the transmit FIFO byte count register (see Table 22 and Section 0)
TXCON, the transmit FIFO control register (see Table 20 and Section 0)
TXFLG, the transmit FIFO flag register (see Table 21 and Section 0)

These registers are endpoint indexed. They are used as a set to control the operation of the transmit

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FIFO, associated with the current endpoint specified by the EPINDEX register (see Table 16 and Section 0).

5.18 Receive FIFOs

The WT65F4 has one receive FIFO for endpoint 0 (See Figure 4). This FIFO is shared with the transmit FIFO. Detail operating is described in section.

5.19 Receive FIFO Features

The receive FIFO is a data buffer with the following features (see Figure 16):

- support for one data set of not greater than eight bytes
- a byte count register accesses the number of bytes in the data set
- flag to signal a full FIFO and an empty FIFO
- capability to re-receive the last data set

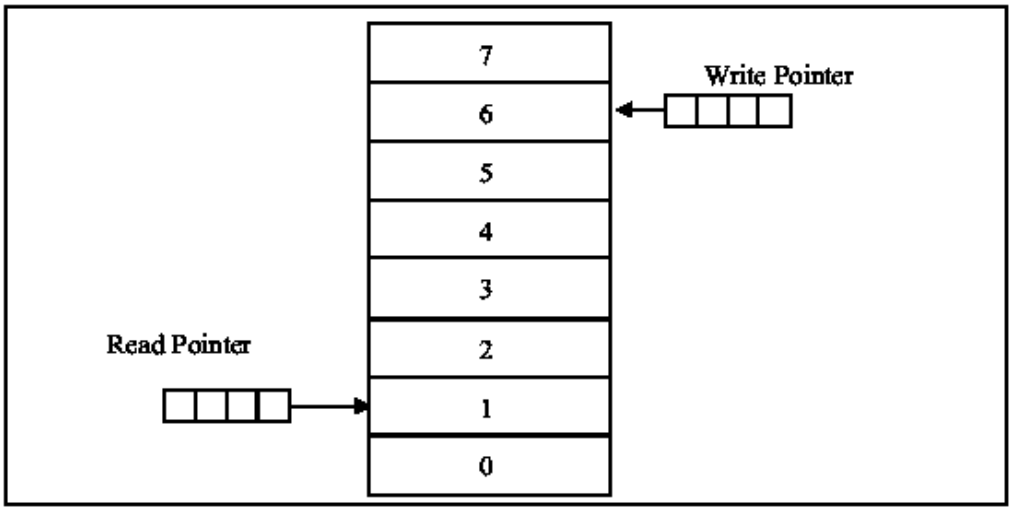

Figure 16. Receive FIFO Outline

The SIL writes to the FIFO location specified by the write pointer also used as the byte-counter to

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indicate how many bytes have been written and not yet read by the 8051 CPU. The write pointer automatically increments by one after a write and decrements by one after a read. The read pointer points the next FIFO location to be read by the 8051 CPU. The read pointer automatically increments by one after a read. The receive FIFO is inhibited to be read by the 8051 CPU when it is empty or before a data set has been successfully written into it. When a SETUP token is detected by the SIL, the SIL flushes the FIFO even if the FIFO is being read by the 8051 CPU.

5.20 Receive Data Set Management

RXFULL = 1 in the RXFLG register (Table 36), indicates the data set has been written into the FIFO and is ready for reception. Following reset, RXFULL = 0 and RXEMP = 1, signifying an empty FIFO. Only the first eight bytes of the data set which size is greater than eight are written into FIFO. RXFULL is however not set until reception is done and successfully acknowledged. RXFULL is cleared by setting the FFRC bit of RXCON (Table 35) in firmware to indicate the data set has

successfully read by CPU. In the case of RXFULL = 1 farther writes to FIFO are ignored. Please note that the content of RXCNT (Table 37) should be read by 8051 CPU to determine the numbers of bytes need to be read Flashmemory FIFO by 8051 CPU. Further reading Flashmemory an empty FIFO is ignored.

Table 10. Status of the receive FIFO data set

RXFULL	RXEMP	Status
0	0	Data set is being written to FIFO
0	1	Empty
1	0	Data set already written to FIFO
1	1	Zero length packet received

When a good reception is completed and the data set has been successfully read by the 8051, firmware must set the FFRC bit of RXCON to advance the write pointer and read pointer to the start point of the FIFO to set up for receiving the next data set. When a bad reception is completed, the write pointer can be reversed to the position of the start point of the FIFO to enable the SIL to re-write the last data set for re-reception. The pointer advance and reversal are accomplished automatically by hardware. Table 11 summarizes how actions following a reception depend on RXERR and RXACK.

Table 11. Truth table for receive FIFO management

RXERR	RXACK	Action at End of Transfer Cycle
0	0	No operation
0	1	Read Pointer and Write Pointer are set to the start point of FIFO when firmware sets the FFRC bit of RXCON
1	0	Write Pointer is set to the start point of FIFO

5.21 Receive FIFO Registers

RXDAT, the receive FIFO data register (see Table 34 and Section 0)
RXCNT, the receive FIFO byte count register (see Table 37 and Section 0)
RXCON, the receive FIFO control register (see Table 35 and Section 0)
RXFLG, the receive FIFO flag register (see Table 36 and Section 0)

These registers are endpoint indexed. They are used as a set to control the operation of the receive FIFO associated with the current endpoint specified by the EPINDEX register (see Table 16 and Section 0).

5.22 Setup Token Receive FIFO Handling

SETUP tokens received by the endpoint zero must be acknowledged, even if the receive FIFO is not empty. As described in section 5.19, when a SETUP token is detected by the SIL, the SIL flushes the FIFO and sets the STOVW bit of RXSTAT (Table 38) for reset and locking the read pointer. These prevent RXURF bit of RXFLG and the read pointer Flashmemory being set if the receive FIFO flush occurs in the middle of an 8051 CPU data read cycle. The STOVW bit is cleared and the EDOVW bit is set when a SETUP packet has been successfully acknowledged. The read pointer will remain locked until both the STOVW and EDOVW bits are cleared. For SETUP packets only, firmware must clear EDOVW before reading data Flashmemory the FIFO. If this is not done, data read Flashmemory the FIFO will be invalid. After processing a SETUP packet, firmware should always check the STOVW and EDOVW flags before setting the RXFFRC bit. When a SETUP packet either has been or is being received, setting of RXFFRC has no effect if either STOVW or EDOVW is set.

5.23 Suspend and Resume

In order to reduce the power consumption, WT65F4 automatically enters the suspend state when it

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has observed no bus traffic for 3 ms. When in suspend, the 8051 CPU and its peripherals are in powerdown mode. Keyboard interrupt is enabled to support remote wakeup. The entire chip consumes less than 100 pA in suspended state.

WT65F4 exits suspend mode when there is bus activity. A USB device may also request the host exits Flashmemory suspend or selective suspend by using electrical signaling to indicate remote wakeup. The ability of a device to signal remote wakeup is optional. WT65F4 allows the host to enable or disable this

capability. Device states are described in Figure 17.

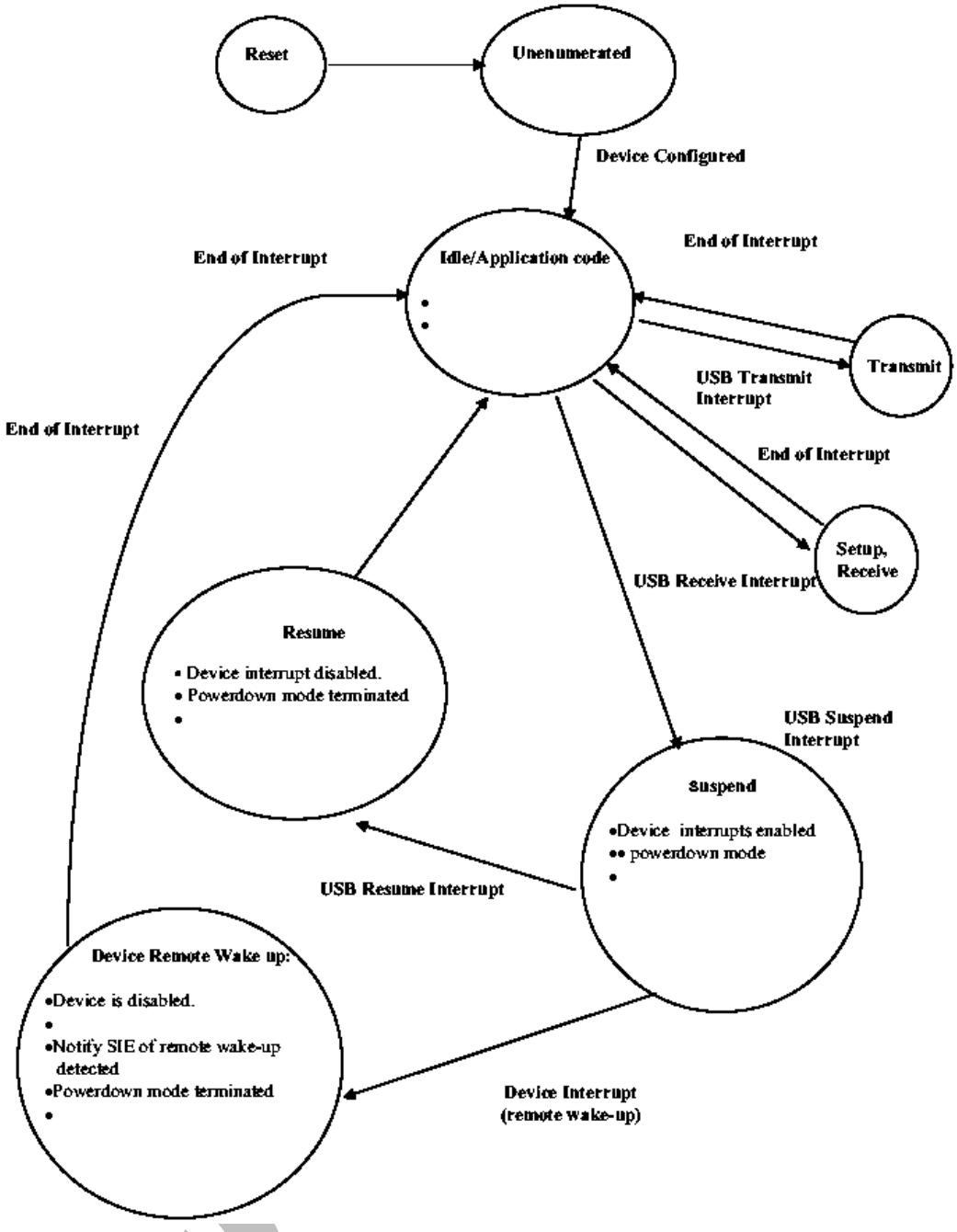

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Figure 17. Suspend and Resume State Diagram

5.24 ISP Mode

Five pins are released for performing ISP mode, they are VDD, GND, RESET, P30/RXD, and P31/TXD. By applying a special pattern through RESET, P30/RXD, and P31/TXD, the device can be forced to enter the ISP mode. The detection of this special pattern is done by firmware. Once the ISP mode is detected, a flag (ISPM) is written to bit 5 of SFR PCON. On the other hand, if ISP mode is not detected after 50 ms, then normal mode is considered. While in the ISP mode, the data and an external clock can be applied via P30/RXD and P31/TXD, respectively. Furthermore, flash IOs are re-routed from normal CPU interface to XFR ISP corresponding registers.

In order to accommodate the system clock variation, it is necessary to build-in the "delay loop" into the ISP program in the 4K ROM. The length of the delay depends on system's clock information notified by PC via P30 and P31.

5.25 ICE Mode

WT65F4 support easy ICE function. Program download, free running and two sets of breakpoint function are supported.

During ICE mode, commands are fed into the device via P4.0 and P4.1. All controls will be done by Weltrend Soft_ICE.

5.26 Normal Download Mode

User can control the Flash-ROM programming in Normal Download mode. When BKEN2 is set by firmware, the Flash IOs are routed from normal CPU interface to four external function registers: ISPCTL, ISPADDL, ISPADDH, and ISPDATA.

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6. External Function Register

FADDR **Address:**

00H

RW **Reset State:**

0000 0000B

Function Address Register. This XFR holds the address for the ISB function.
During bus enumeration, it is written with a unique value assigned by the host.

Table 12. Function Address Register (FADDR,00H)

7							**0**
---							**ADR6:0**

Bit Number	Bit Mnemonic	Function
7	**---**	**Reserved:** **Write zero to this bit**
6:0	**ADR6:0**	**7-bit Programmable Function Address:** **This register is programmed through the commands Received via endpoint 0 on configuration, which should be** **the only time the firmware should change the value of this** **Register. This register is hardware read-only .**

USBI **Address:**

01H

RW (Read to clear) **Reset State:**

xx00 0000B

Table 13. USB Interrupt Register (USBI,01H)

7							**0**

- - -		RESUME	SUSPEND	USBRx0INT	USBTx2INT	USBTx1INT	USBTx0INT

Bit Number	Bit Mnemonic	Function
5	RESUME	USB SIE has detected a RESUME signaling on the USB lines. This interrupt is used to terminate the powerdown mode.
4	SUSPEND	USB SIE has detected a SUSPEND signaling on the USB lines. The corresponding ISR should put the whole chip into powerdown mode.
6	USBRx0INT	Function Receive Done Flag for endpoint 0.
2	USBTx2INT	Function Transmit Done Flag for endpoint 2.
1	USBTx1INT	Function Transmit Done Flag for endpoint 1.
0	USBTx0INT	Function Transmit Done Flag fir endpoint 0.

USBKAIE **Address:** **02H**

RW **Reset State:** **0000 0000B**

USB/Keyboard/AD Interrupt Enable Register.

Table 14. USB/Keyboard/AD Interrupt Enable Register (USBKAIIE, 02H)

7 **0**

KINT_IE	ADINT_IE	RESUME_IE	SUSPEND_IE	Rx0INT_IE	Tx2INT_IE	Tx1INT_IE	Tx0INT_IE

Bit Number	Bit Mnemonic	Function

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7	KINT_IE	Keyboard Interrupt Enable: Enable Keyboard Interrupt (KEYINT). Firmware can set this bit before entering the powerdown or idle mode to enable remote wakeup. operation.
6	ADINT_IE	External2 Interrrupt Enable: Enable External2 Interrupt EXT2INT
5	RESUME_IE	RESUME Interrupt Enable.
4	SUSPEND_IE	SUSPEND Interrupt Enable.
3	Rx0INT_IE	Function Transmit Done Interrupt Enable 0: Enable receive done interrupt for endpoint 0 (USBTx0INT).
2	Tx2INT_IE	Function Transmit Done Interrupt Enable2: Enable receive done interrupt for endpoint 2 (USBTx0INT).
1	Tx1INT_IE	Function Transmit Done Interrupt Enable 1: Enable receive done interrupt for endpoint 1 (USBTx0INT).
0	Tx0INT_IE	Function Transmit Done Interrupt Enable 0: Enable receive done interrupt for endpoint 0 (USBTx0INT).

For all bits, a ‘1’ means the interrupt is enabled and will cause an interrupt to be Signaled to the microcontroller. A ‘0’ means the associated interrupt source is Disabled and cannot cause an interrupt.

SIEI **Address:**

03H

RW **Reset State:**

Xx00 0000B

USB SIE Interface Register.

Table 15. USB SIE Interface Register (SIEI,03H)

7 **0**

- - -	- - -	LVREN	CLK12MEN	V33EN	USBSTREN	DMEN	WAKEUP

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Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Values read Flashmemory these bits are indeterminate. Write zeros to these bits.
5	LVREN	0: LVR is disabled 1: LVR is enabled
4	CLK12MEN	0: USB clock source comes from 6MHz X'tal. 1: USB clock source comes from 12MHz X'tal.
3	V33EN	0: 3.3V regulator circuits turned off and low voltage reset circuit disabled. 1: 3.3V Regulator circuits turned on and low voltage reset circuit enabled.
2	USBRSTEN	USB Reset enable. Firmware can set this bit to enable /disable USB Reset.
1	DMEN	0: USB 1.5k-ohm resisters turn off. 1: USB 1.5k-ohm resisters turn on.
0	WAKEUP	This bit is used to initiate a remote wakeup. Set by firmware to drive resume signaling on the USB lines to the host or upstream hub. Cleared by hardware when resume signaling is done.

EPINDEX

Address: **05H**

RW

Reset State: **xxxx xx00B**

Endpoint Index Register. This Register identifies the endpoint pair. Its contents select the transmit and receive FIFO pair and serve as an index to endpoint-specific XFRs.

Table 16. Endpoint Index Register (EPINDEX,05H)

7						0	
---	---	---	---	---	---	EPINX1	EPINX0

Bit	Bit	Function

Number	Mnemonic	
7:2	---	Reserved : Values read Flashmemory these bits are indeterminate. Write zeros to these bits.
1:0	EPINX1:0	Endpoint Index: 00 = Function Endpoint 0. 01 = Function Endpoint 1 10 = Function Endpoint 2. 11 = Function Endpoint 3.

The value in this register selects the associated bank of endpoint-indexed XFRs Including TXDAT, TXCON, TXFLG, TXCNT, TXSTAT, RXDAT, RXCON, RXFLG, RXCNT, RXSTAT and EPCON.

EPCON **Address: 06H**

(Endpoint-indexed) Reset State: Endpoint 0: 001x0101B

RW **Endpoint 1,2: x0xx xx00B**

Endpoint Control Register. This XFR configures the operation of the endpoint specified by EPINDEX.

Table 17. Endpoint Control Register (EPCON,06H)

7							0
RXSTL	TXSTL	CTLEP	---	RXIE	RXEPEN	TXOE	TXEPEN

Bit Number	Bit Mnemonic	Function
7	RXSTL	Stall Receive Endpoint: Set this bit to stall the receive endpoint . Clear this bit

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		only when the host has intervened through commands sent down endpoint 0. When this bits is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is set and RXSETUP is set, the receive endpoint will NAK. This bit does not affect the reception of SETUP token by a control endpoint.
6	TXSTL	Stall Transmit Endpoint: Set this bit to stall the transmit endpoint. This bit should be cleared only when the host has intervened through commands sent down endpoint 0. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid IN token. When this bit is set and RXSETUP is set, the receive endpoint will NAK.
5	CTLEP	Control Endpoint: Set this bit to configure the endpoint as a control endpoint. Only control endpoint is capable of receiving SETUP tokens.
4	---	Reserved: Value read Flashmemory this bit is indeterminate. Write zero to this bit.

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Bit Number	Bit Mnemonic	Function
3	RXIE	Receive Input Enable: Set this bit to enable data Flashmemory the USB to be written into the receive FIFO. If cleared, the endpoint will not write the receive data into the receive FIFO and at the end of reception, but will return a NAK handshake on a valid OUT token if the RXSTL bit is not set. This bit does not affect a valid SETUP token. A valid SETUP token and packet overrides this bit if it is cleared, and place the receive data in the FIFO.
2	RXEPEN	Receive Endpoint Enable: Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to valid OUT or SETUP token. This bit is hardware read-only and has the highest priority among RXIE and RXSTL. Note that endpoint 0 is enabled for reception upon reset.
1	TXOE	Transmit Output Enable: This bit is used to enable the data in TXDAT to be transmitted. If cleared, the endpoint returns a NAK handshake to a valid IN token if the TXSTL bit is not set.
0	TXEPEN	Transmit Endpoint Enable: This bit is used to enable the transmit endpoint. When disabled, the endpoint does not response to a valid IN Token. This bit is hardware read only. Note that endpoint 0 is enabled for transmission upon reset.

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SPWDCTL **Address:**
07H
W **Reset State:**
0000 0010B

Enable or Disable Watch-dog timer function. Watch-dog timer will generate a reset pulse if CPU does not write any data to CLRWDT register for more than 2^{22} clock cycles (CPU clock). This function could be disabled by clearing EN_WDT bit.

Table 18. Speaker/Watch-dog Timer Control Register (SPWDCTL,07H)

7 **0**

SPKON	DUALT	---	---	---	---	EN_WDT	WDTRST

Bit Number	Bit Mnemonic	Function
7	SPKON	1: ADPCM push-pull DA function enable. PWM disabled 0: PWM function enabled. ADPCM push-pull DA disabled
6	DUALT	1: Dual-tone. Combine SPKENV0 and SPKENV1 0: Mono-tone. Select only spkenv0
5:2	---	Reserved: Values read Flashmemory these bits are indeterminate. Write zeros to these bits.
1	EN_WDT	1: Enable Watch-dog timer 0: Disable Watch-dog timer
0	WDTRST	0: No Watch-dog timer reset 1: Generate a pulse to clear the Watch-dog timer

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TXDAT **Address:**
08H
W (Endpoint-indexed) **Reset State: xxxx**
xxxxB

Transmit FIFO Data Register. Data to be transmitted by the FIFO specified by EPINDEX is first written to this register.

Table 19.Transmit FIFO Data Register (TXDAT, 08H)

7							**0**
TXDAT7:0							

Bit Number	Bit Mnemonic	Function
7:0	TXDAT7:0	Transmit Data Bytes (write-only) To write data to the transmit FIFO, write to this register. The write pointer is incremented automatically after a write.

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TXCON **Address:**
09H
W (Endpoint-indexed) **Reset State: 0xxx**
xxxxB

Transmit FIFO Control Register. Controls the transmit FIFO specified by EPINDEX.

Table 20.Transmit FIFO Control Register (TXCIN, 09H)

7							**0**
TXCLR	---	---	---	---	---	---	---

Bit Number	**Bit Mnemonic**	**Function**
7	TXCLR	Transmit Clear: Setting this bit flushes the transmit FIFO, resets all the read/write pointers, sets the EMPTY bit in TXFLG, and clears all other bits in TXFLG. After the flush, hardware clears this bit.
6:0	---	Reserved: Values read Flashmemory these bits are indeterminate. write zeros to these bits.

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TXFLG **Address:**
0AH
RW(Write 0 to clear)(Endpoint-indexed) **Reset State: xxxx**
1000B

Transmit FIFO Flag Register. These flags indicate the status of data packets in the transmit FIFO specified by EPINDEX.

Table 21. Transmit FIFO Flag Register (TXFLG,0AH)

7							**0**
SPKON	DUALT	---	---	---	---	EN_WDT	WDTRST

Bit Number	**Bit Mnemonic**	**Function**
7:4	---	Reserved: Values read Flashmemory these bits are Indeterminate. Write zeros to these bits.
3	TXEMP	Transmit FIFO Empty Flag (read-only): Hardware sets this bit when the data set has been read out of the transmit FIFO by SIL. Hardware clears this bit when the empty condition no longer exists. This bit always tracks the current transmit FIFO status. This flag is also set when a zero-length data packet is transmitted.
2	TXFULL	Transmit FIFO Full Flag (read-only): This flag indicates the data set is present in the transmit FIFO. This bit is set after write to TXCNT to reflect the condition of the data set. Hardware clears this bit when the data set has been successfully transmitted.
1	TXURF	Transmit FIFO Underrun Flag (read-, clear-only)*: Hardware sets this flag when an addition byte is read Flashmemory an empty transmit FIFO. This is a sticky bit that must be cleared through firmware by writing a ‘0’ to this bit .When the transmit FIFO underruns, the read

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		pointer will not advance—it remains locked in the empty position.
0	TXOVF	Transmit FIFO Overrun Flag (read-, clear-only)*: This bit is set when an additional byte is written to a FIFO with TXFULL = 1. This is a sticky bit that must be

		cleared through firmware by writing a '0' to this bit . When the transmit FIFO overruns, the write pointer will not advance – it remains locked in the full position.

Note (*) : When set, all transmission are NAKed.

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TXCNT **Address:**
0BH
RW (Endpoint-indexed) **Reset State: 0000**
0000B

Transmit FIFO Byte Count Register. This register stores the number of bytes for the data packet in the transmit FIFO specified by EPINDEX.

Table 22. Transmit FIFO Bytes Count Register (TXCNT, 0BH)

7 **0**

---	---	---	---	**TXCNT 3:0**

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Write zeros to these bits.
3:0	TXCNT 3:0	Transmit Byte Count (write-only): The number of bytes in the data set being written to the transmit FIFO. When this register is written, TXFULL is set. Write the byte count to this register after writing data set to TXDAT.

To send a status stage after a control write or no data control command or a null packed, write 0 to TXCNT.

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TXSTAT **Address: 0CH**

RW(Write 0 to clear)(Endpoint-indexed) **Reset State: 0000 0000B**

Endpoint Transmit Status Register. Contains the current endpoint status of the transmit FIFO specified by EPINDEX.

Table 23. Endpoint Transmit Status Register (TXSTAT, 0CH)

7							0
TXSEQ	---	---	---	---	TXVOID	TXERR	TXACK

Bit Number	Bit Mnemonic	Function
7	TXSEQ	Transmit Current Sequence Bit (read-only): This bit will be transmitted in the next PID and toggled on a valid ACK handshake. This bit is toggled by hardware on a valid SETUP token.
6:3	---	Reserved: Write zeros to these bits.
2	TXVOID	Transmit Void (read-only): A void condition has occurred in response to a valid IN token. Transmit void is closely associated with the NAK/STALL handshake returned by the function after a valid IN token, due to the conditions that cause the Transmit FIFO to be unable or not ready to transmit. Use this bit to check any NAK/STALL handshake returned by the function. This bit does not affect the USBTxxINT, TXERR or TXACK bit. This bit is updated by hardware at the end of a non-isochronous transaction in response to a valid IN token.
1	TXERR	Transmit Error (read-only): An error condition has occurred with the transmission. Complete or partial data has been transmitted. The error can be one if the following: Data transmitted successfully but no handshake received.

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		Transmit FIFO goes into underrun condition while transmitting. The corresponding transmit done bit is set when active. This bit is updated by hardware along with the TXACK bit at the end of data transmission (this bit is mutually exclusive with TXACK).

Bit Number	Bit Mnemonic	Function
0	TXACK	Transmit Acknowledge (read-only): Data transmission completed and acknowledged successfully. The corresponding transmit done bit is set when active. This bit is updated by hardware along with the TXERR bit at the end of data transmission (this bit is mutually exclusive with TXERR)

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PWM0 **Address:**
0DH
W **Reset State: 0000**
0000B

PWM0 Duty Control Register

Table 24. Pwm0 Duty Control Register (PWM, 0DH)

7 **0**

PWM07	PWM06	PWM05	PWM04	PWM03	PWM02	PWM01	PWM00

Bit Number	Bit Mnemonic	Function
7:3	PWM07 PWM06 PWM05 PWM04 PWM03	Select 0/32 to 31/32 duty cycle & extended pulse 00000: duty cycle = 0 00001: duty cycle = 1/32 00010: duty cycle = 2/32 …. 11110: duty cycle = 30/32 11111: duty cycle = 31/32
2:0	PWM02 PWM01 PWM00	The corresponding PWM register controls the PWM duty cycle. Duty cycle range is from 0/32 to 31/32. LSB 3-bit of PWM register determines which frame will be extended two Tosc. 000 : no extended pulse. 001 : extend two Tosc at frame 4. 010 : extended two Tosc at frame 2 and 6. 011 : extended two Tosc at frame 2, 4and 6. 100 : extended two Tosc at frame 1, 3, 5and 7. 101 : extended two Tosc at frame 1, 3, 4, 5and 7. 110 : extended two Tosc at frame 1, 2, 3, 5, 6and 7. 111 : extended two Tosc at frame 1, 2, 3, 4, 5, 6 and 7.

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PWM1 **Address:**
0EH
W **Reset State: 0000**
0000B

PWM1 Duty Control Register

Table 25. PWM1 Duty Control Register (PWM1, 0EH)

7 **0**

PWM17	PWM16	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10

Bit Number	Bit Mnemonic	Function
7:3	PWM17 PWM16 PWM15 PWM14 PWM13	Select 0/32 to 31/32 duty cycle & extended pulse 00000: duty cycle = 0 00001: duty cycle = 1/32 00010: duty cycle =2/32 …. 11110: duty cycle = 30/32 11111: duty cycle = 31/32
2:0	PWM12 PWM11 PWM10	The corresponding PWM register controls the PWM duty cycle. Duty cycle range is from 0/32 to 31/32. LSB 3-bit of PWM register determines which frame will be extended two Tosc. 000 : no extended pulse. 001 : extend two Tosc at frame 4. 010 : extended two Tosc at frame 2 and 6. 011 : extended two Tosc at frame 2, 4and 6. 100 : extended two Tosc at frame 1, 3, 5and 7. 101 : extended two Tosc at frame 1, 3, 4, 5and 7. 110 : extended two Tosc at frame 1, 2, 3, 5, 6and 7. 111 : extended two Tosc at frame 1, 2, 3, 4, 5, 6 and 7.

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P2ODCTL **Address:**
0FH
W **Reset State: 0000**
0000B

Strong Current Source Control for Port 20~27.

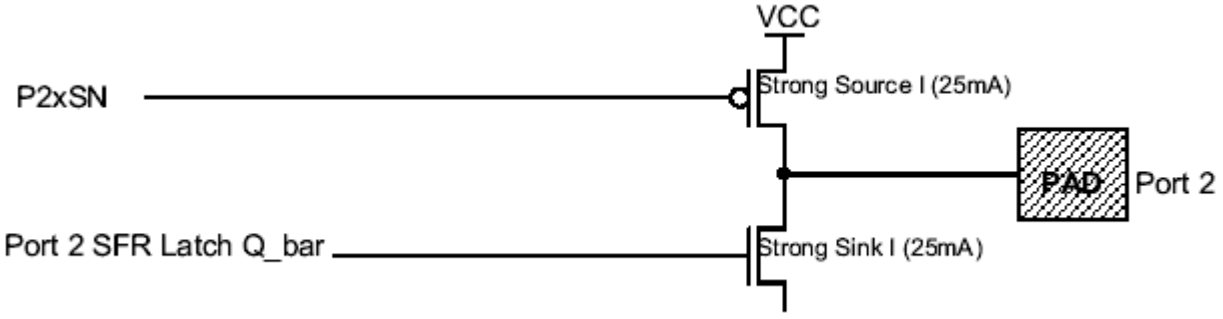
Table 26. Port2 Current Control Register (P2ODCTL, 0FH)

7 **0**

--	--	P25SN	P24SN	--	--	P21SN	P20SN

Bit Number	Bit Mnemonic	Function
7:0	-- -- P25SN P24SN -- -- P21SN P20SN	Default value is '00000000' (strong current source turned off). When '1' is written to one if the bits, the corresponding strong current source is turned on.

As shown in Figure 18, the strong source current PMOS can be turned on or off (open drain circuit). Open drain circuit is selected when P2xSN is set to high in order to turn on the corresponding PMOS.



ISP
11H

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W **Reset State: xxxx**
xxxxB

Program Data to Flash for ISP function.

Table 27. ISP program control Register (ISP_CTL, 11H)

7 **0**

XE	YE	SE	OE	ERASE	MAS1	PROG	NVSTR

Bit Number	Bit Mnemonic	Function
0	NVSTR	Defines non-volatile store cycle.
1	PROG	Defines program cycle.
2	MAS1	Defines mass erase cycle, erase whole block.
3	ERASE	Defines erase cycle.
4	OE	Output enable, tri-state DOUT when OE=0.
5	SE	Sense amplifier enable.
6	YE	Y address enable, YMUX is disabled when YE=0.
7	XE	X address enable, all rows are disabled when XE=0.

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ISPADDL **Address:**
12H
W **Reset State: xxxx**
xxxxB

Address Low byte to Flash for ISP function.

Table 28. ISP Address low byte Register (ISPADDL, 12H)

7 **0**

---	**---**	**---**	**YADR 4/ A4**	**YADR 3/ A3**	**YADR 2/ A2**	**YADR 1/ A1**	**YADR 0/ A0**

Bit Number	Bit Mnemonic	Function
5:0	YADR[7:0]/ A[4:0]	Address bus bit 0 to 4 (which indicates YADR 0 to 4)

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ISPADDH **Address:**
13H
W **Reset State: xxxx**
xxxxB

Address high byte to Flash for ISP function.

Table 29. ISP Address high byte Register (ISPADDH, 13H)

7 **0**

YADR 7/ A12	YADR 6/ A11	YADR 5/ A10	YADR 4/ A9	YADR 3/ A8	YADR 2/ A7	YADR 1/ A6	YADR 0/ A5

Bit Number	Bit Mnemonic	Function
7:0	YADR[7:0]/ A[12:5]	Address bus bit 5 to 12 (which indicates XADR 0 to 7)

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ISPDATA **Address:**
14H
RW **Reset State: xxxx**
xxxxH

Program Data to Flash for ISP function.

Table 30. ISP program data Register (ISPDATA, 14H)

7 **0**

D7	D6	D5	D4	D3	D2	D1	D1

Bit Number	Bit Mnemonic	Function
7:0	D	Program data bus to flash during ISP function

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ADPWM_C **Address:**
15H
W **Reset State: 0000**
0000B

AD/PWM function control.

Table 31. AD/PWM function control Register (ADPWM_C, 15H)

7 **0**

ADON	ADEN	ADSEL2	ADSEL1	ADSEL0	ADref	PWMEN1	PWMEN0

Bit Number	Bit Mnemonic	Function
0	PWMEN0	0: Disable channel 0 PWM function 1: Enable channel 0 PWM function
1	PWMEN1	0: Disable channel 1 PWM function 1: Enable channel 1 PWM function
2	ADref	0: Select VDD to be the reference voltage of ADC circuit 1: Select ADvref (P07) pin as the reference input voltage of ADC circuit
5:3	ADSEL[2:0]	000: Selected AD0 input pin 001: Selected AD1 input pin 010: Selected AD2 input pin 011: Selected AD3 input pin 100: Selected AD4 input pin 101: Selected AD5 input pin 110: Selected AD6 input pin 111: Selected AD7 input pin
6	ADEN	0: Disable ADC function 1: Enable ADC function
7	ADON	0: Disable ADC for power-down mode 1: Enable ADC for power-down mode

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ADCLK **Address:**
16H
W **Reset State: x000**
0000B

ADC Sample clock control register.

Table 21. Transmit FIFO Flag Register (TXFLG,0AH)

7 **0**

--	--	--	--	--	ADCLK2	ADCLK1	ADCLK0

Bit Number	Bit Mnemonic	Function
7	--	Reserved
6:5	--	Reserved
4:3	--	Reserved
2:0	ADCLK	000: AD clock=Fosc/2 (used for 8051 clock=0.5MHz) 001: AD clock=Fosc/4 (used for 8051 clock=1MHz) 010: AD clock=Fosc/8 (used for 8051 clock=2MHz) 011: AD clock=Fosc/16 (used for 8051 clock=4MHz) 100: AD clock=Fosc/32 (used for 8051 clock=6, 8MHz) 101: AD clock=Fosc/48 (used for 8051 clock=10~12MHz)

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KYADI **Address:**
17H
RW(Read to clear) **Reset State: 00xx**
xxxxB

Kayboard/AD Interrupt Register. Contains Keyboard and ADC interrupt flags. A '1' Indicates that an interrupt is actively pending. All bits are cleared after a read.

Table 33. Kayborad/AD Interrupt Register (KYADI, 17H)

7							0
KEY INT	AD IN T	---	---	---	---	---	---

Bit Number	Bit Mnemonic	Function
7	KEYINT	Keyboard Interrupt Flag. This bit is set when any Keyboard Input pin (K10~K17) is low. This interrupt is used To wake-up CPU from powerdown mode or idle mode. In Normal operation, this interrupt is can also be set from External interrupt pins.
6	ADINT	A/D converter interrupt flag. This bit is set when the A/D data was converted.
5:0	---	Reserved: Values read Flashmemory these bits are indeterminate. Write zeros to these bits.

KYADI register can be read by CPU even if KINT_IE and ADINT_IE bits in USBKAIE (02h) are not enabled.

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RXDAT **Address:**
18H
R **Reset State: xxxx**
xxxxB

Receive FIFO Data Register. Receive FIFO data specified by EPINDEX is stored And read Flashmemory this register.

Table 34. Receive FIFO Data Register (RXDAT, 18H)

7							**0**
RXDAT7:0							

Bit Number	Bit Mnemonic	Function
7:0	RXDAT7:0	Receive Data Byte (read-only): To write data to the receive FIFO, the SIL writes to this register. To read data Flashmemory the receive FIFO, the 8051 CPU reads Flashmemory this register. The write pointer and read pointer are incremented automatically after a write and read, respectively.

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RXCON **Address:**
19H
W **Reset State: 0xx0**
xxxxB

Receive FIFO Control Register. Controls the receive FIFO.

Table 35. Receive FIFO Control Register (RXCON, 19H)

7							**0**
RXCLR	**---**	**---**	**RXFFRC**	**---**	**---**	**---**	**---**

Bit Number	**Bit Mnemonic**	**Function**
7	RXCLR	Clear the Receive FIFO: Set this bit to flush the entire receive FIFO. All flags in RXFLG revert to their reset states (RXEMP is set; all other flags clear). Hardware clears this bit when the flush operation is complete.
6:5	---	Reserved: Values read Flashmemory these bits are indeterminate. Write zeros to these bits.
4	RXFFRC	FIFO Read Complete: Set this bit to release the receive FIFO when a data set read is complete. Setting this bit clears the RXFULL bit (in the RXFLG register) corresponding to the data set that was just read. Hardware clears this bit after the RXFULL bit is cleared. All data Flashmemory this data set must have been read. Note that FIFO Read Complete only works if STOVW and EDOVW are cleared.
3:0	---	Reserved: Values read Flashmemory these bits are indeterminate. Write zeros to these bits.

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RXFLG

Address:

1AH

RW(Write 0 to clear)

Reset State: xxxx

1000B

Receive FIFO Flag register. These flags indicate the status of data packets in the Receive FIFO.

Table 36. receive FIFO Flag Register (RXFLG, 1AH)

7 **0**

---	---	---	---	RXEMP	RXFULL	RXURF	RXOVF

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Values read Flashmemory these bits are indeterminate. Write zeros to these bits.
3	RXEMP	Receive FIFO Empty Flag (read-only): Hardware sets this bit when the data set has been read out of the receive FIFO. Hardware clears this bit when the empty condition no longer exists. This is not a sticky bit and always tracks the current status. This flag is also set when a zero-length packet is received.
2	RXFULL	Receive FIFO Full Flag (read-only): This flag indicates the data set is present in the receive FIFO. Hardware sets this bit when the data set has been successfully received. This bit is cleared after write to RXCNT to reflect the condition of the data set. Likewise, this bit is cleared after setting of the RXFFRC bit.
1	RXURF	Receive FIFO Underrun Flag (read-, clear-only)*: Hardware sets this bit when an additional byte is read Flashmemory an empty receive FIFO. This bit is cleared through firmware by writing a '0' to this bit When the receive FIFO underruns, the read pointer will not advance – it remains locked in the empty position.

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0	RXOVF	Receive FIFO Overrun Flag (read-, clear-only)*: This bit is set when the SIL writes an additional byte to a receive FIFO with RXFULL = 1. This is a sticky bit that must be cleared through firmware by writing a '0' to this bit, although it can be cleared by hardware if a SETUP packed is received after an RXOVF error had already occurred. When the receive FIFO overruns, the write pointer will not advance – it remains locked in the full position.

* When set, all transmission are NAKed.

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RXCNT **Address:**
1BH
W **Reset State: 0000**
0000B

Receive FIFO Byte Count Register. This register is used to store the number of byte For the data packed received in the receive FIFO specified by EPINDEX.

Table 37. Receive FIFo Byte Count Register (RXCNT, 1BH)

7 **0**

---	---	---	---	**RXCNT3:0**

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Always zeros.
3:0	RXCNT3:0	Byte Count (read-only): The number of bytes in data set being written to the receive FIFO. When this register is written, RXFULL is not set until reception is successfully acknowledged. After the SIL writes a data set to the RXFIFO, it writes the byte count to this register. The 8051 CPU reads the byte count Flashmemory this register to determine how many bytes to read Flashmemory the RXFIFO.

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RXSTAT **Address:**
1CH
RW(Write 0 to clear) **Reset State: 0000**
0000B

Endpoint Receive Status Register. Contains the current endpoint status of the receive FIFO specified by EPINDEX.

Table 38. Endpoint Receive Status Register (RXSTAT, 1CH)

7 **0**

RXSEQ	RXSETUP	STOVW	EDOVW	---	RXVOID	RXERR	RXACK

Bit Number	Bit Mnemonic	Function
7	RXSEQ	Receive Endpoint Sequence Bit (read-only): This bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit will be set (or created) by hardware after reception of SETUP token.
6	RXSETUP	Receive Setup Token (read-, clear-only): This bit is set by hardware when a valid SETUP token has been received. When set, this bit causes received IN or OUT token to be NAKED until the bit is cleared to allow a control transaction. IN or OUT token is NAKed even if the endpoint is stalled (RXSTL or TXSTL) to allow a control transaction to clear a stalled endpoint. Clear this bit upon detection of a SETUP token after the firmware is ready to complete the setup stage of control transaction.
5	STOVW	Start Overwrite Flag (read-only); Set by hardware upon receipt of SETUP token for any control endpoint to indicate that the receive FIFO is being overwritten with new SETUP data. When set, the FIFO state (RXFULL and read pointer) resets and is locked for this endpoint until EDOVW is set. This prevents a prior, ongoing firmware read Flashmemory corrupting the read pointer as the receive FIFO is being cleared and new data is being written into it. This bit is cleared by hardware at the end of handshake phase transmission of the setup stage. This bit is used only for control endpoint.

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4	EDOVM	End Overwrite Flag (read-, clear-only): This flag is set by hardware during the handshake phase of a SETUP stage. It is set after every SETUP packet is received and must be cleared prior to reading the contents of the FIFO. When set, the FIFO state (RXFULL and read pointer) remains locked for this endpoint until this bit is cleared. This prevents a prior, ongoing firmware read Flashmemory corrupting the read pointer after the new data has been written into the receive FIFO. This bit is only used for control endpoint. Note: Make sure the EDOVW bit is cleared prior to reading the contents of the receive FIFO.
3	---	Reserved: write zero to this bit.
2	RXVOID	Receive Void Condition (read-only): This bit is set when no valid data is received in response to a SETUP or OUT token due to one of the following conditions: 1. The receive FIFO is still locked. 2. The EPCON register RXSTL bit is set. This bit is set and cleared by hardware. This bit is updated by hardware at the end of the transaction in response to a valid OUT token.
1	RXERR	Receive Error (read-only): Set when an error condition has occurred with the reception. Complete or partial data has been written into the receive FIFO. No handshake is returned. The error can be one of the following conditions: 1. Data failed CRC check. 2. Bit stuffing error. 3. A receive FIFO goes into overrun or underrun condition while receiving. This bit is updated by hardware at the end of a valid SETUP or OUT token transaction. The corresponding receive done bit is set when active. This bit is updated with the RXACK bit at the end of data reception and is mutually exclusive with RXACK.
0	RXACK	Receive Acknowledged (read-only): This bit is set when data is received completely into a receive FIFO and an ACK handshake is sent. This read-only bit is updated by hardware at the end of valid SETUP or OUT token transaction. The corresponding

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		receive done bit set when active. This bit is updated with the RXERR bit at the end of data reception and is mutually exclusive with RXERR.

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ADL **Address:**
1DH
R **Reset State: 0000**
0000B

ADC Lower Byte Data.

Table 39. ADC Lower Byte Data Register (ADL, 1DH)

7 **0**

ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0

Bit Number	Bit Mnemonic	Function
7:0	ADB	ADC Data lower byte

ADH **Address:**
1EH

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R **Reset State: 0000**
0000B

ADC Higher Byte Data Register.

Table 40. ADC Higer Byte Data Register (ADH, 1EH)

7 **0**

---	---	---	---	AD B11	AD B10	AD B9	AD B8

Bit Number	Bit Mnemonic	Function
3:0	ADB	ADC Data higher byte [11:8]

SPKENV0 **Address:**
10H
W **Reset State:**

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0000 0000B

Push-pull DA speaker output envelope Register.

Table 41. Push-pull DA speaker output envelope (spkenv0, 10H)

7							**0**
SPKENV0							

Bit Number	**Bit Mnemonic**	**Function**
7:0	SPKENV0	Push-pull DA speaker output envelope

SPKENV1 **Address:**
1FH
W **Reset State: 0000**
0000B

Push-pull DA speaker output envelope Register.

Table 42. Push-pull DA speaker output envelope (SPKENV1, 1FH)

7							**0**
SPKENV1							

Bit Number	**Bit Mnemonic**	**Function**

7:0	SPKENV 1	Push-pull DA speaker output envelope

7. AC and DC Electrical Characteristics

Table 43. DC Electrical Characteristics

(VCC=5V± 5%, GND=0V, TA=0~70℃, F_{OSC}=6MHz, unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
V_{DD}	Supply Voltage		2.7	--	5.5	V
V_{IH}	Input High Voltage		0.7 V_{DD}	--	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	--	0.3 V_{DD}	V
V_{OH}	Output High Voltage (Port 0)	I_{OH}= -25mA	V_{DD}-0.1	--	V_{DD}	V
V_{OH}	Output High Voltage (Port 1~3)	I_{OH}= -80uA	2.4	--	--	V
V_{OL}	Output Low Voltage (Port 0)	I_{OL}=25mA	0	--	0.4	V
V_{OL}	Output Low Voltage (port 1~3)	I_{OL}= 1.6mA	--	--	0.45	V
I_{IL}	Input Leakage Current	0V<V_{IN}<V_{DD}	-1	--	1	μ

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						A
R_{PH}	Pull High Resistance			25		Kohm
$I_{DD,OPT}$	Operating Current	F_{OSC}= 6MHz, No load			2	mA
$I_{DD,IDL}$	Idle Mode Current	F_{OSC}= 6MHz, No load V3.3 regulator and 1.5K register turn off			200	uA
$I_{DD,PD}$	Power Down Mode Current	Oscillator disabled. No Load, V3.3 regulator and 1.5K register turn off			1	μA
V33	4. 3V regulator output		3.0	3.3	3.6	V
V_{RESET}	Reset Voltage$_{note}$		3.5	3.6	3.7	V

Note: Reset voltage only valid when USB function is used.

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Table 44. Absolute Maximum Rating

DC supply voltage	-0.3V to +7.0V
Input / Output voltage	GND - 0.3V to VCC + 0.3V
Operating ambient temperature	-0℃ to + 7℃
Storage temperature	-25℃ to + 125℃
Operating voltage (VCC)	+2.7V to 5.5V

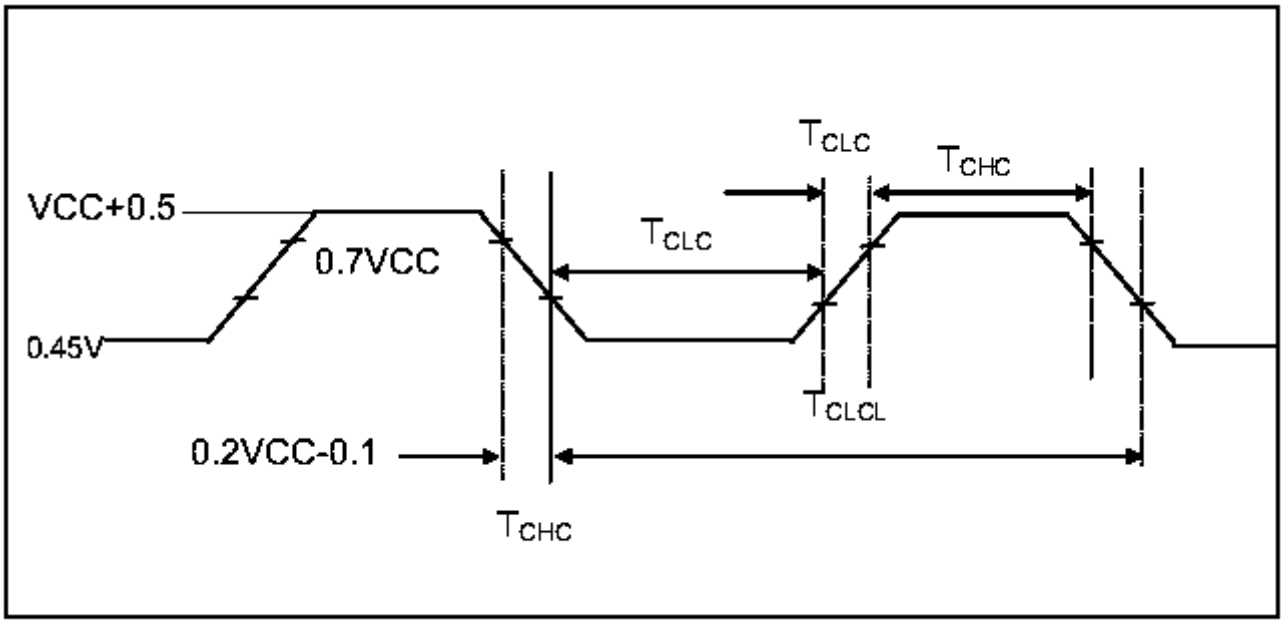

Figure 19. External Clock Drive Waveform

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Table 45. AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
$1/T_{CLCL}$	Oscillator frequency	5.94	6.06	MHz
T_{CHCX}	High time	$0.35T_{CLCL}$	$0.65T_{CLCL}$	nS
T_{CLCX}	Low time	$0.35T_{CLCL}$	$0.65T_{CLCL}$	nS
T_{CLCH}	Rise time		20	nS
T_{CHCL}	Fall time		20	nS
T_{POR}	Power on reset internal High time	30		μS

Note : 10KΩ pullup resistor, C= 50pF