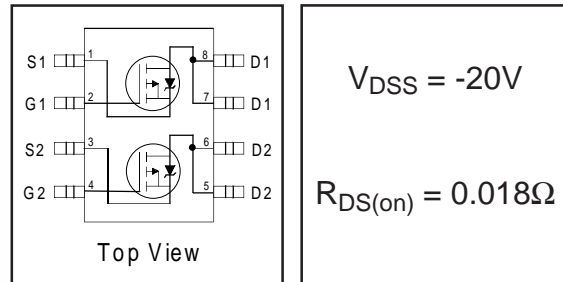


IRF7324

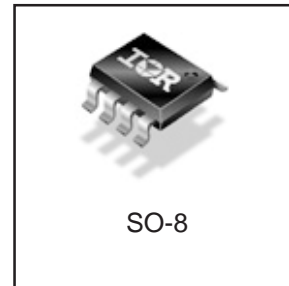
HEXFET[®] Power MOSFET

- Trench Technology
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Low Profile (<1.1mm)
- Available in Tape & Reel
- 2.5V Rated



Description

New trench HEXFET[®] Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in battery and load management applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	-20	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -4.5\text{V}$	-9.0	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -4.5\text{V}$	-7.1	
I_{DM}	Pulsed Drain Current ^①	-71	
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation ^③	2.0	W
$P_D @ T_A = 70^\circ\text{C}$	Maximum Power Dissipation ^③	1.3	W
	Linear Derating Factor	16	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

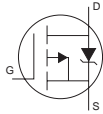
Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ^③	62.5	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.02	—	V/°C	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.018	Ω	$V_{GS} = -4.5V, I_D = -9.0A$ ②
		—	—	0.026		$V_{GS} = -2.5V, I_D = -7.7A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.45	—	-1.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	19	—	—	S	$V_{DS} = -10V, I_D = -9.0A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	42	63	nC	$I_D = -9.0A$
Q_{gs}	Gate-to-Source Charge	—	7.1	11		$V_{DS} = -16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	12	18		$V_{GS} = -5.0V$
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = -10V$
t_r	Rise Time	—	36	—		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	170	—		$R_G = 6.0\Omega$
t_f	Fall Time	—	190	—		$R_D = 10\Omega$ ②
C_{iss}	Input Capacitance	—	2940	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	630	—		$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance	—	420	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-71		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -2.0A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	180	270	ns	$T_J = 25^\circ\text{C}, I_F = -2.0A$
Q_{rr}	Reverse Recovery Charge	—	300	450	nC	$di/dt = -100A/\mu s$ ②

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ③ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

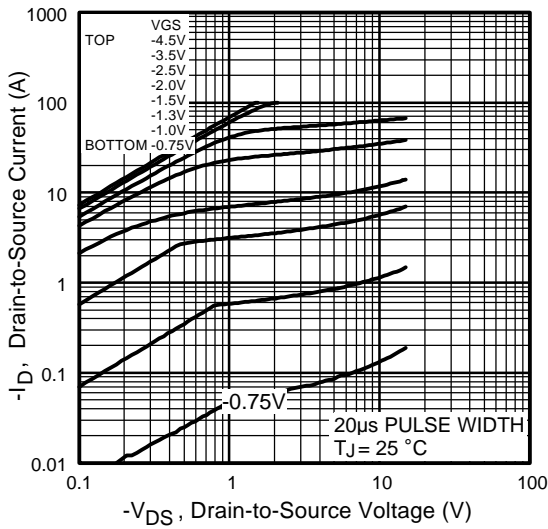


Fig 1. Typical Output Characteristics

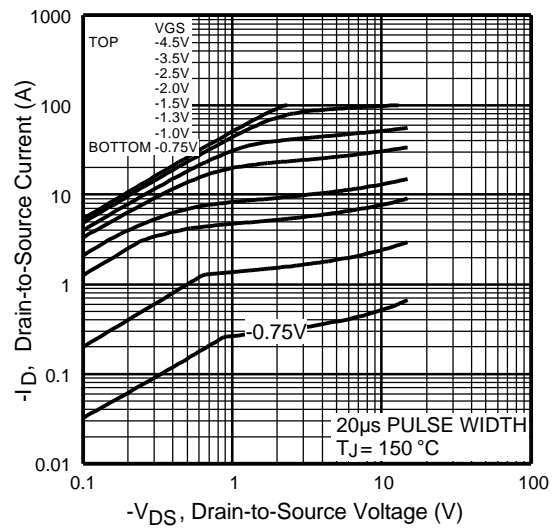


Fig 2. Typical Output Characteristics

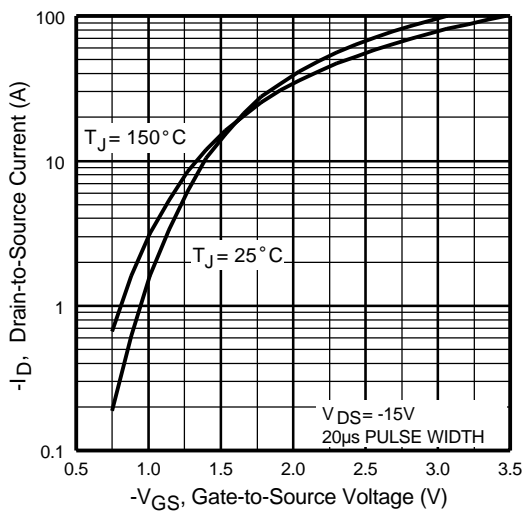


Fig 3. Typical Transfer Characteristics

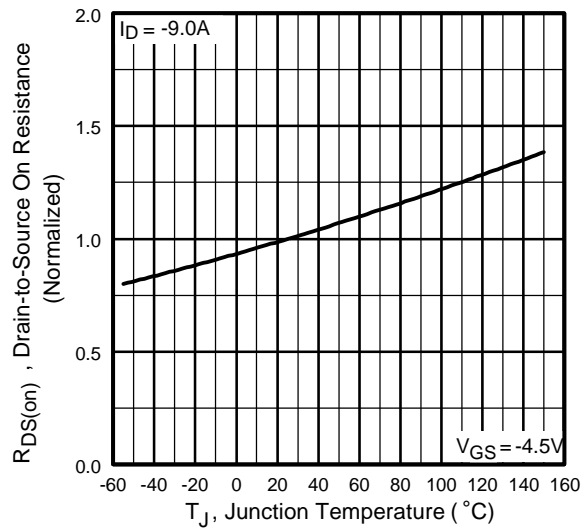


Fig 4. Normalized On-Resistance Vs. Temperature

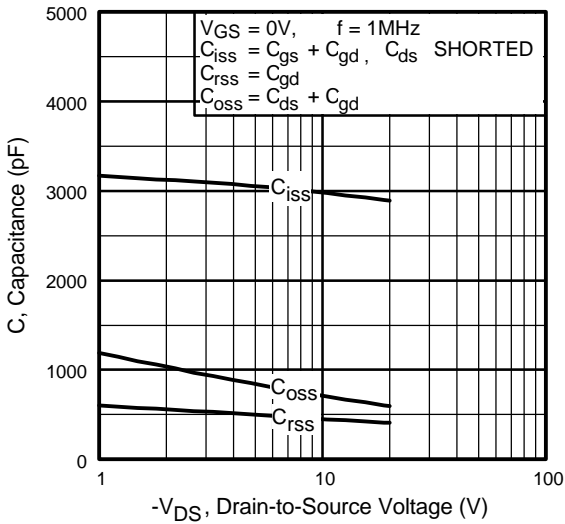


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

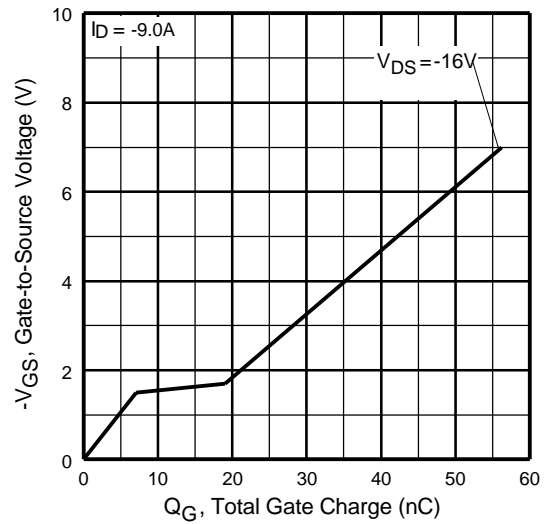


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

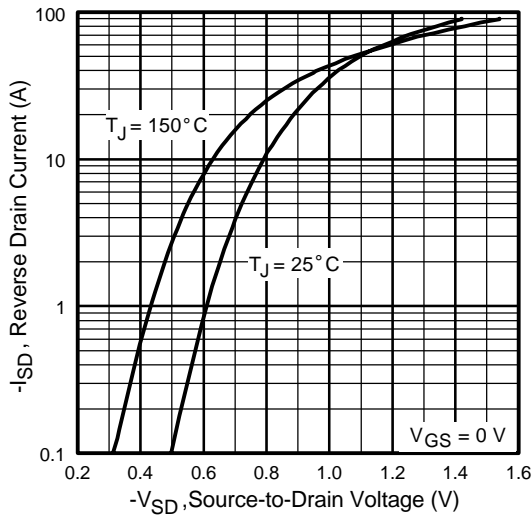


Fig 7. Typical Source-Drain Diode Forward Voltage

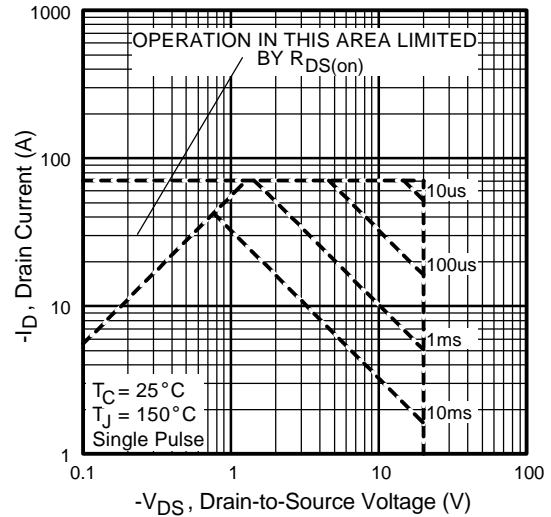


Fig 8. Maximum Safe Operating Area

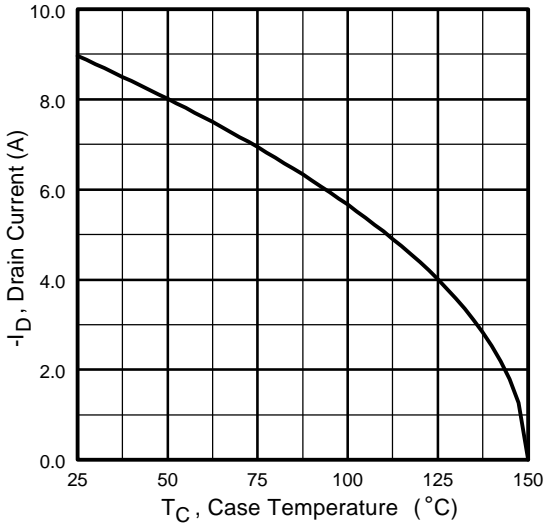


Fig 9. Maximum Drain Current Vs. Case Temperature

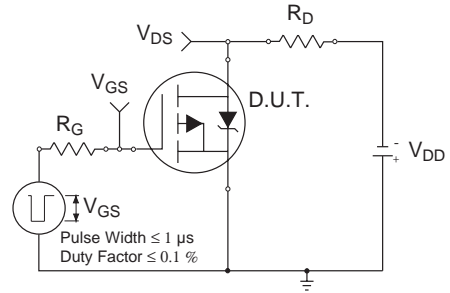


Fig 10a. Switching Time Test Circuit

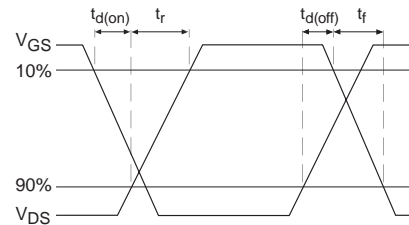


Fig 10b. Switching Time Waveforms

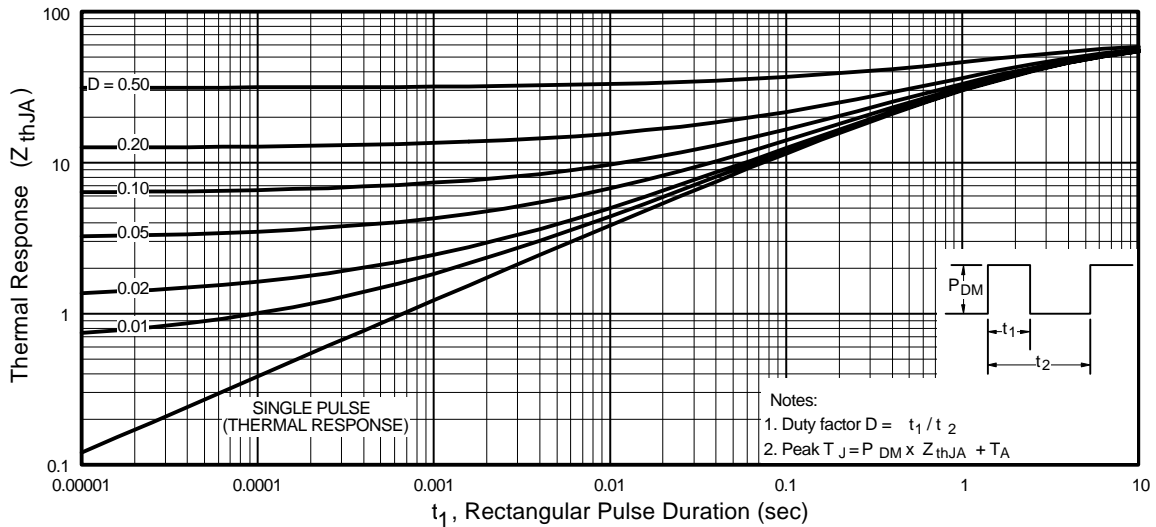


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

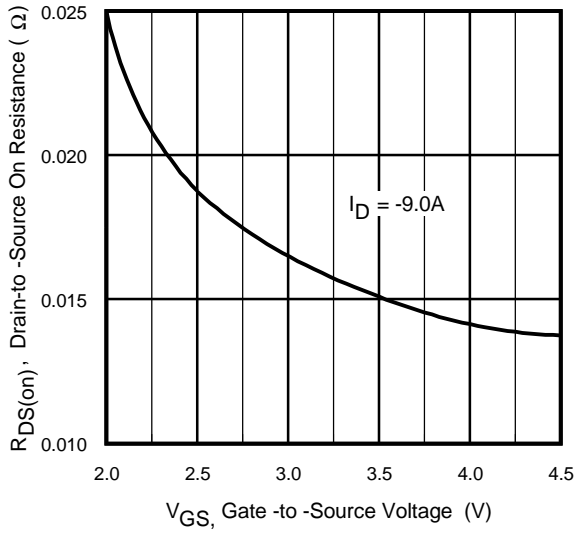


Fig 12. Typical On-Resistance Vs. Gate Voltage

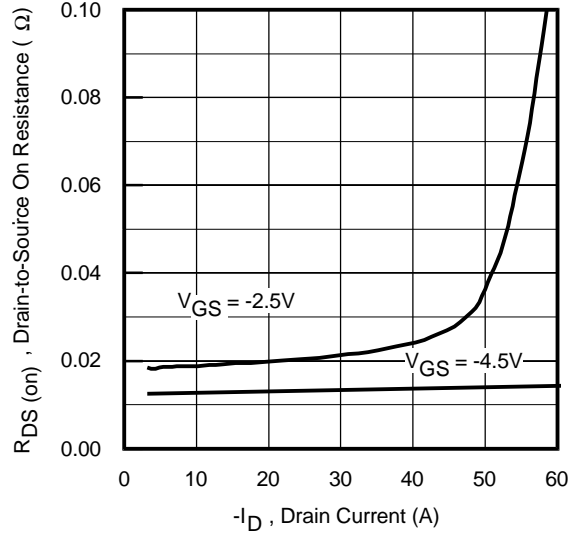


Fig 13. Typical On-Resistance Vs. Drain Current

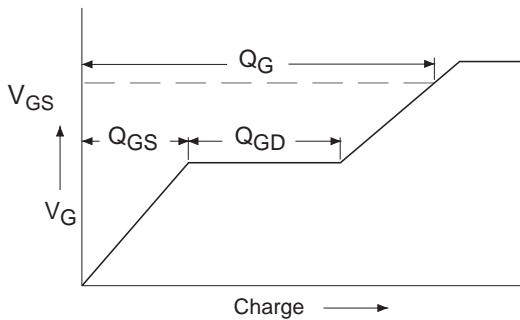


Fig 14a. Basic Gate Charge Waveform

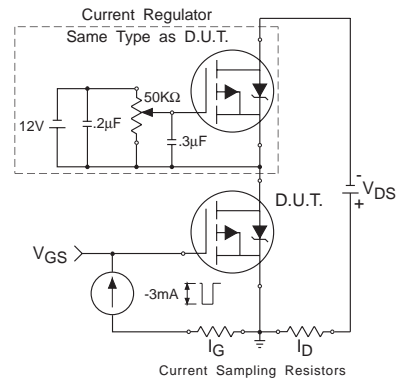
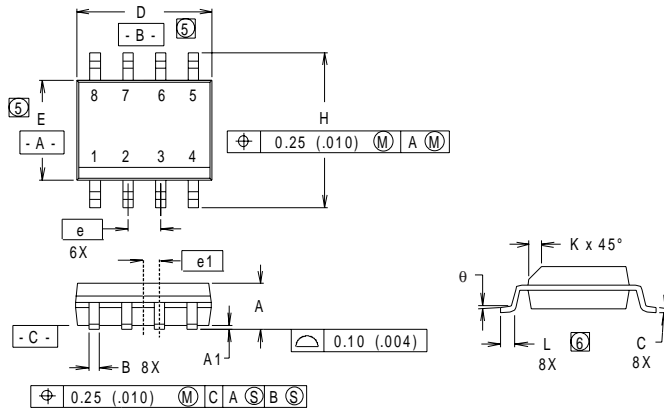


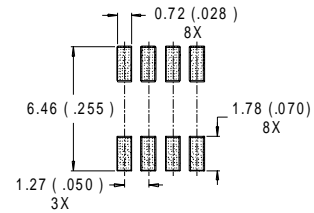
Fig 14b. Gate Charge Test Circuit

SO-8 Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT

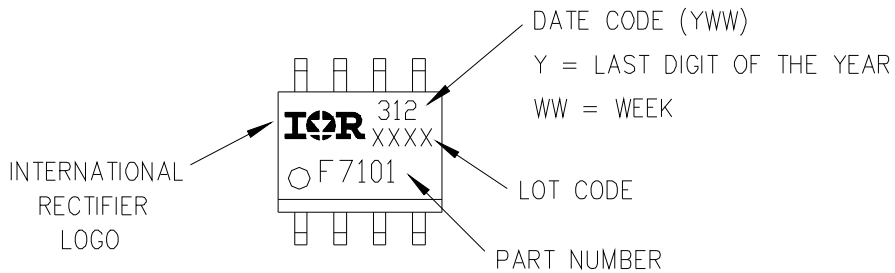


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
6. DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

Part Marking

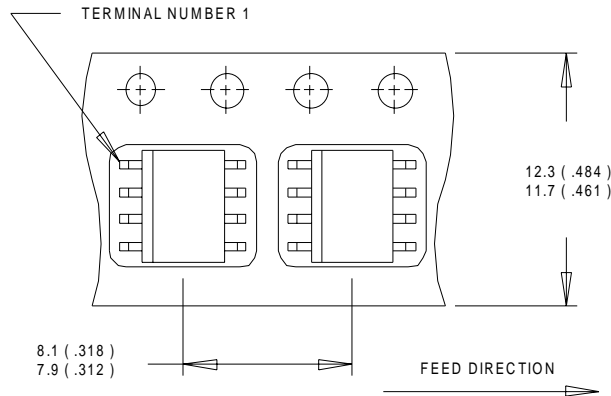
EXAMPLE: THIS IS AN IRF7101



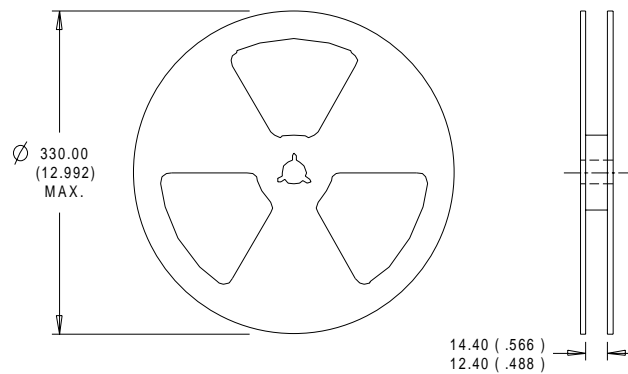
IRF7324

International
IR Rectifier

Tape and Reel



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

International
IR Rectifier

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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

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Data and specifications subject to change without notice. 2/00