

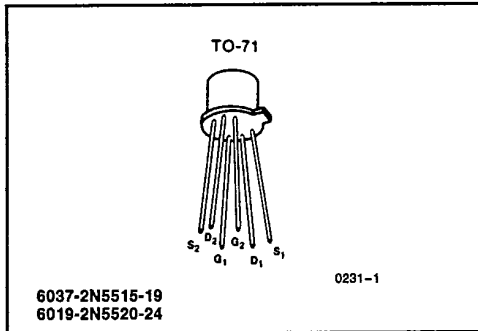


**2N5515-2N5524**  
**Dual N-Channel JFET**  
**Low Noise Amplifier**

**FEATURES**

- Tight Temperature Tracking
- Tight Matching
- High Common Mode Rejection
- Low Noise

**PIN CONFIGURATION**



**ABSOLUTE MAXIMUM RATINGS**

( $T_A = 25^\circ\text{C}$  unless otherwise specified)  
 Gate-Source or Gate-Drain Voltage ..... -40V  
 Gate Current (Note 1) ..... 50mA  
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+200^\circ\text{C}$   
 Operating Temperature Range .....  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead Temperature (Soldering, 10sec) .....  $+300^\circ\text{C}$

	One Side	Both Sides
Power Dissipation ( $T_A = 85^\circ\text{C}$ )	250mW	375mW
Derate above $25^\circ\text{C}$	2.0mW/ $^\circ\text{C}$	3.0mW/ $^\circ\text{C}$

**NOTE:** Per transistor.  
**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING INFORMATION**

TO-72
2N5515
2N5516
2N5517
2N5518
2N5519
2N5520
2N5521
2N5522
2N5523
2N5524

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units
$I_{GSS}$	Gate Reverse Current	$V_{GS} = -30\text{V}, V_{DS} = 0$		-250	pA
		$T_A = 150^\circ\text{C}$		-250	nA
$BV_{GSS}$	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-40		V
$V_P$	Gate-Source Pinch-Off Voltage	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$	-0.7	-4	
$I_{DSS}$	Drain Current at Zero Gate Voltage (Note 1)	$V_{DS} = 20\text{V}, V_{GS} = 0$	0.5	7.5	mA
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	$f = 1\text{kHz}$	1000	4000	$\mu\text{s}$
$g_{oss}$	Common-Source Output Conductance			10	
$C_{rss}$	Common-Source Reverse Transfer Capacitance (Note 3)		$f = 1\text{MHz}$		5
$C_{iss}$	Common-Source Input Capacitance (Note 3)			25	

INTERMIL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

*NOTE: All typical values have been characterized but are not tested*

**2N5515-2N5524**

INTERSIL

T-29-27

2N5515-2N5524

**ELECTRICAL CHARACTERISTICS** (Continued) ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units	
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 3)	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$	f = 10Hz		30	nV/ $\sqrt{\text{Hz}}$
					15	
					10	
$I_G$	Gate Current	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		-100	pA	
			$T_A = 125^\circ\text{C}$	-100	nA	
$V_{GS}$	Gate Source Voltage		-0.2	-3.8	V	
$g_{fs}$	Common-Source Forward Transconductance (Note 1)	f = 1kHz	500	1000	$\mu\text{s}$	
$g_{oss}$	Common-Source Output Conductance			1	$\mu\text{s}$	

**MATCHING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$I_{DSS1}/I_{DSS2}$	Drain Current Ratio at Zero Gate Voltage (Note 1)	$V_{DS} = 20\text{V}, V_{GS} = 0$	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	
$ I_{G1} - I_{G2} $	Differential Gate Current (+125°C)	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		10		10		10		10		10	nA
$g_{fs1}/g_{fs2}$	Transconductance Ratio (Note 1)	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	
$ g_{oss1} - g_{oss2} $	Differential Output Conductance	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$		0.1		0.1		0.1		0.1		0.1	$\mu\text{s}$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		5		5		10		15		15	mV
$\Delta V_{GS1} - V_{GS2} $ $\Delta T$	Gate-Source Voltage Differential Drift ( $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ )	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		5		10		20		40		80	$\frac{\mu\text{V}}{^\circ\text{C}}$
CMRR	Common Mode Rejection Ratio (Note 2, 3)	$V_{DD} = 10$ to $20\text{V}, I_D = 200\mu\text{A}$	100		100		90						dB

NOTES: 1. Pulse duration of 28ms used during test.  
 2. CMRR =  $20 \log_{10} \Delta V_{DD} / \Delta |V_{GS1} - V_{GS2}|$ , ( $\Delta V_{DD} = 10\text{V}$ )  
 3. For design reference only, not 100% tested.

10

INTERSIL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.