MC10E196, MC100E196

5V ECL Programmable Delay Chip

The MC10E/100E196 is a programmable delay chip (PDC) designed primarily for very accurate differential ECL input edge placement applications.

The delay section consists of a chain of gates and a linear ramp delay adjust organized as shown in the logic symbol. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80 ps. These two elements provide the E196 with a digitally-selectable resolution of approximately 20 ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

The FTUNE input takes an analog voltage and applies it to an internal linear ramp for reducing the 20 ps L.S.B. minimum resolution still further. The FTUNE input is what differentiates the E196 from the E195.

An eighth latched input, D7, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 2.0 ns Worst Case Delay Range
- ≈20 ps/Delay Step Resolution
- Linear Input for Tighter Resolution
- >1.0 GHz Bandwidth
- On Chip Cascade Circuitry
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 425 devices

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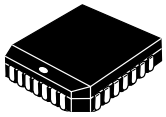
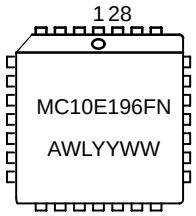
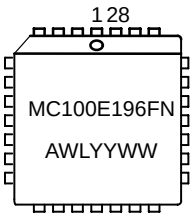
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776





A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E196FN	PLCC–28	37 Units/Rail
MC10E196FNR2	PLCC–28	500 Units/Reel
MC100E196FN	PLCC–28	37 Units/Rail
MC100E196FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT

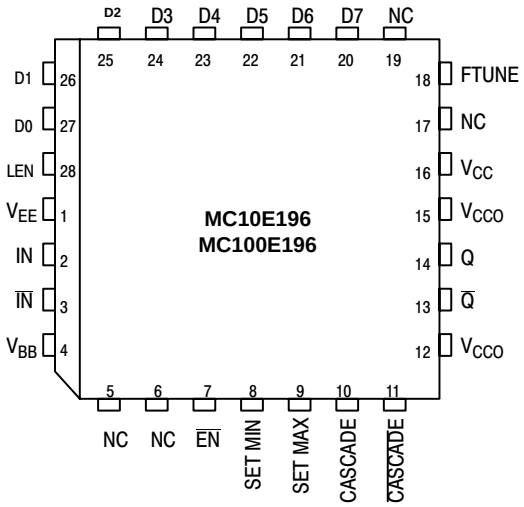


Figure 1. Pinout: 28-Lead PLCC
(Top View)

* All V_{CC} and V_{CCO} pins are tied together on the die.

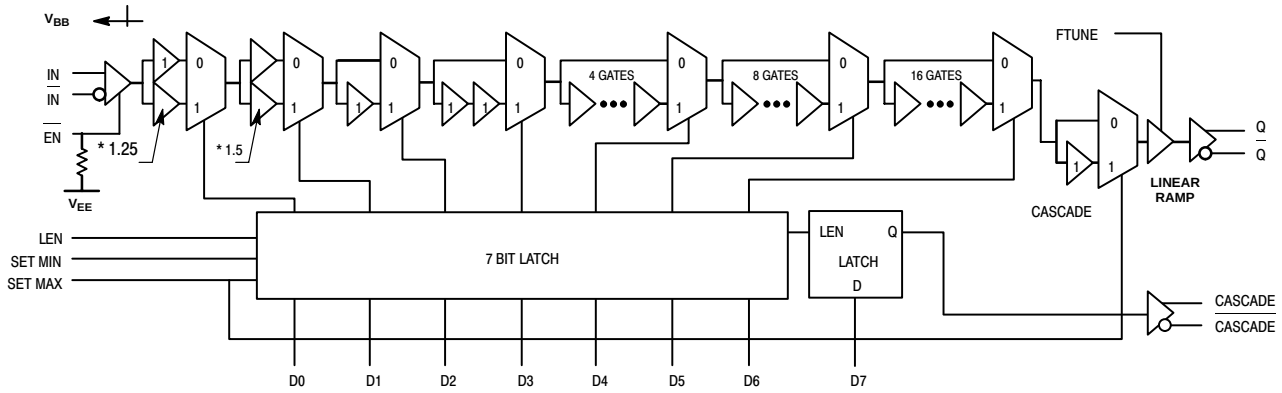
Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
IN/$\overline{IN}$	ECL Signal Input
$\overline{EN}$	ECL Input Enable (H Forces Q Low)
D[0:7]	ECL Mux Select Inputs
Q/$\overline{Q}$	ECL Signal Output
LEN	ECL Latch Enable
SET MIN	ECL Min Delay Set
SET MAX	ECL Max Delay Set
CASCADE	ECL Cascade Signal
FTUNE	ECL Linear Voltage Input
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

TRUTH TABLE

$\overline{EN}$	L	Q = IN
$\overline{EN}$	H	Q Logic Low
LEN	L	Pass Through D[0:10]
LEN	H	Latch D[0:10]
SETMIN	L	Normal Mode
SETMIN	H	Min Delay Path
SETMAX	L	Normal Mode
SETMAX	H	Max Delay Path



* DELAYS ARE 25% OR 50% LONGER THAN STANDARD (STANDARD ≈ 80 PS)

Figure 2. LOGIC DIAGRAM – SIMPLIFIED

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 2)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 3)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
3. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 5)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 6)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 6)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
6. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 8)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		130	156		130	156		150	179	mA
V_{OH}	Output HIGH Voltage (Note 9)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 9)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 10)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
9. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 11)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		130	156		130	156		150	179	mA
V_{OH}	Output HIGH Voltage (Note 12)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 12)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
12. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
13. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

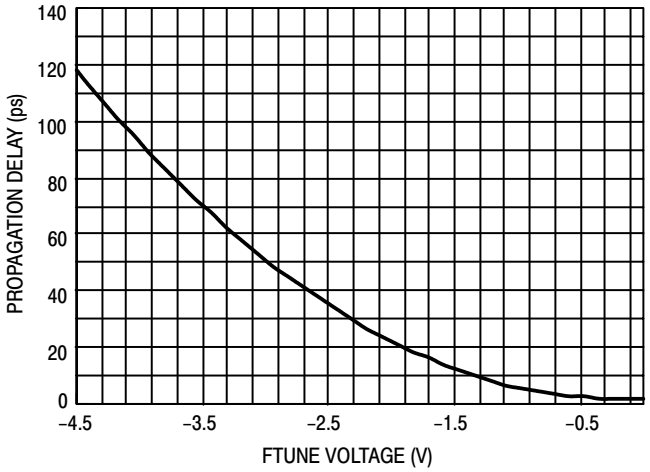
AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 14)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		TBD			>1.0			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay										ps
	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765	
	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720	
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950	
	D7 to CASCADE	300	450	700	300	450	700	300	450	700	
t_{RANGE}	Programmable Range										ps
	t_{PD} (max) – t_{PD} (min)	2000	2175		2050	2240		2375	2580		
Δt	Step Delay (Note 20)										ps
	D0 High		17			17.5			21		
	D1 High		34			35			42		
	D2 High	55	68	105	55	70	105	65	84	120	
	D3 High	115	136	180	115	140	180	140	168	205	
	D4 High	250	272	325	250	280	325	305	336	380	
	D5 High	505	544	620	515	560	620	620	672	740	
	D6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450	
Lin	Linearity (Note 21)	D1	D0		D1	D0		D1	D0		
t_{SKEW}	Duty Cycle Skew										ps
	t_{PHL}–t_{PLH} (Note 15)		±30			±30			±30		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_s	Setup Time										ps
	D to LEN	200	0		200	0		200	0		
	D to IN (Note 16)	800			800			800			
	$\overline{EN}$ to IN (Note 17)	200			200			200			
t_h	Hold Time										ps
	LEN to D	500	250		500	250		500	250		
	IN to $\overline{EN}$ (Note 18)	0			0			0			
t_R	Release Time										ps
	$\overline{EN}$ to IN (Note 19)	300			300			300			
	SET MAX to LEN	800			800			800			
	SET MIN to LEN	800			800			800			
t_{jit}	Jitter (Note 22)		<5.0			<5.0			<5.0		ps
t_r t_f	Output Rise/Fall Time										ps
	20–80% (Q)	125	225	325	125	225	325	125	225	325	
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650	

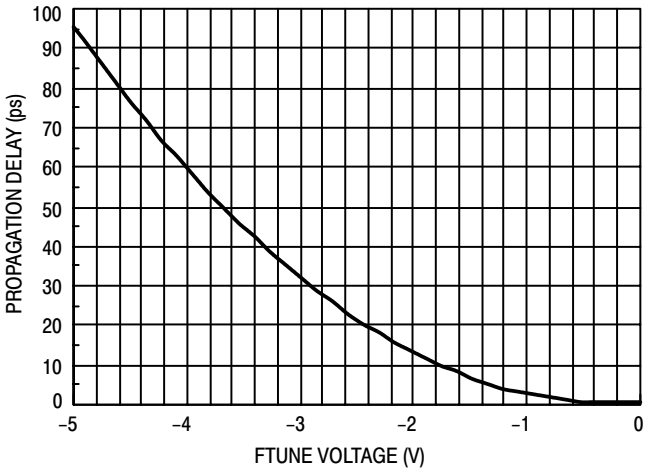
14. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
    100 Series: V_{EE} can vary +0.46 V / –0.8 V.
15. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
16. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
17. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
18. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/IN transition.
19. This release time is the minimum time that $\overline{EN}$ must be de–asserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
20. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
21. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs Dn). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
22. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

ANALOG INPUT CHARACTERISTICS

Ftune = V_{CC} to V_{EE}



Propagation Delay versus Ftune Voltage (100E196)



Propagation Delay versus Ftune Voltage (10E196)

USING THE FTUNE ANALOG INPUT

The analog FTUNE pin on the E196 device is intended to add more delay in a tunable gate to enhance the 20 ps resolution capabilities of the fully digital E195. The level of resolution obtained is dependent on the number of increments applied to the appropriate range on the FTUNE pin.

To provide this further level of resolution (See Logic Diagram), the FTUNE pin must be capable of adjusting the additional delay finer than the 20 ps digital resolution. From the provided graphs one sees that this requirement is easily achieved as over the entire FTUNE voltage range a 100 ps additional delay can be achieved. This extra analog range ensures that the FTUNE pin will be capable even under worst case conditions of covering the digital resolution.Typically the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, the graphs provided should be used. As an example if a tuning range of 40 ps is selected to cover worst case conditions and ensure coverage of the digital range, from the 100E196 graph a voltage range of –3.25 V to –4.0 V would be necessary on the FTUNE pin. Obviously there are numerous voltage ranges which can be used to cover a given delay range, users are given the flexibility to determine which one best fits their designs.

Cascading Multiple E196's

To increase the programmable range of the E196 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E196's without the need for any external gating. Furthermore this capability requires only one more address line per added E196. Obviously cascading multiple PDC's will result in a larger programmable range, however, this increase is at the expense of a longer minimum delay.

Figure 3 illustrates the interconnect scheme for cascading two E196's. As can be seen, this scheme can easily be expanded for larger E196 chains. The D7 input of the E196 is the cascade control pin. With the interconnect scheme of Figure 3 when D7 is asserted it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0–A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A0–A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E196 device. When D7 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0–A6 address bus. Chip #1 on the other hand will have its SET

MAX pin asserted resulting in the device delay to be independent of the A0–A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E196.

When cascading multiple PDC's it will prove more cost effective to use a single E196 for the MSB of the chain while using E195 for the lower order bits. This is due to the fact that only one fine tune input is needed to further reduce the delay step resolution.

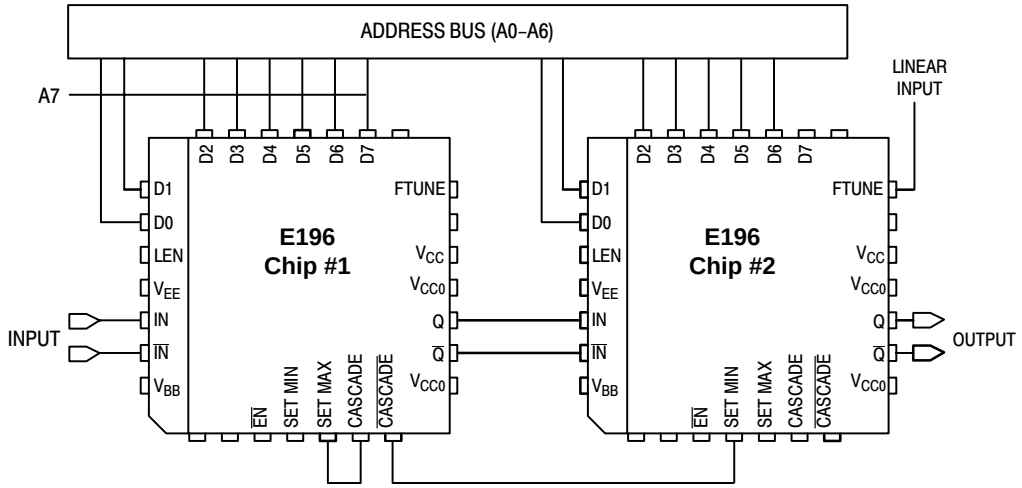


Figure 3. Cascading Interconnect Architecture

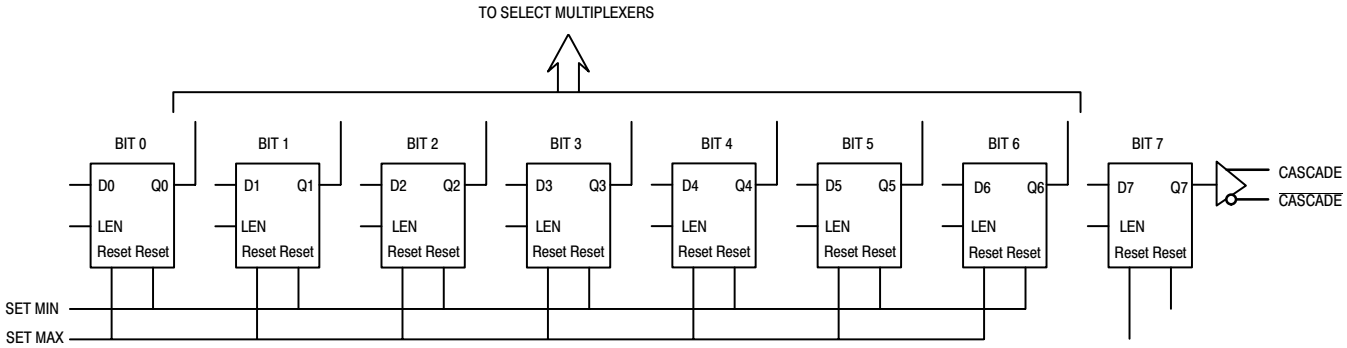


Figure 4. Expansion of the Latch Section of the E196 Block Diagram

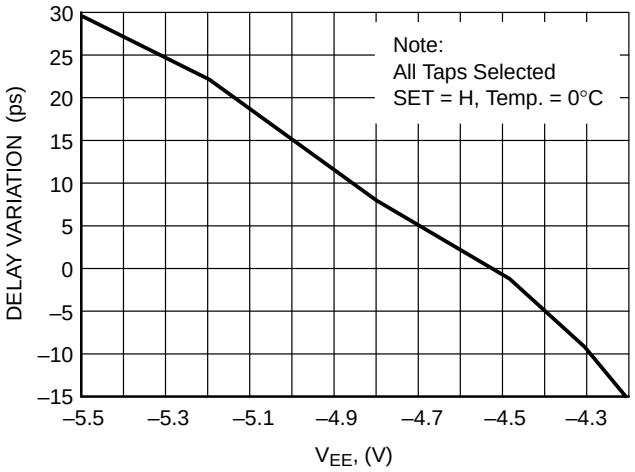


Figure 5. Change in Delay vs. Change in Supply Voltage

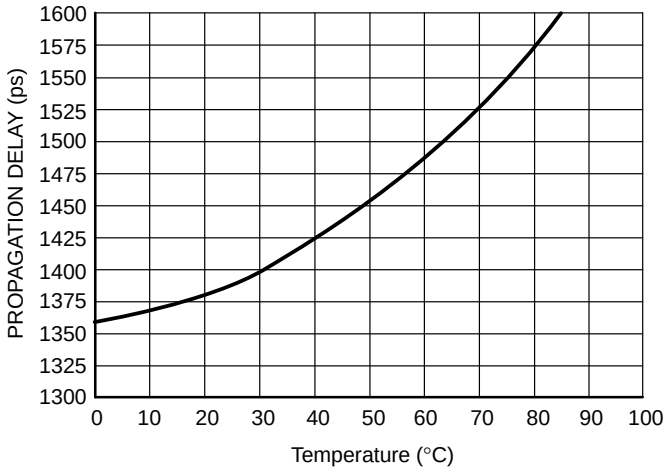


Figure 6. Delay vs. Temperature (Fixed Path)

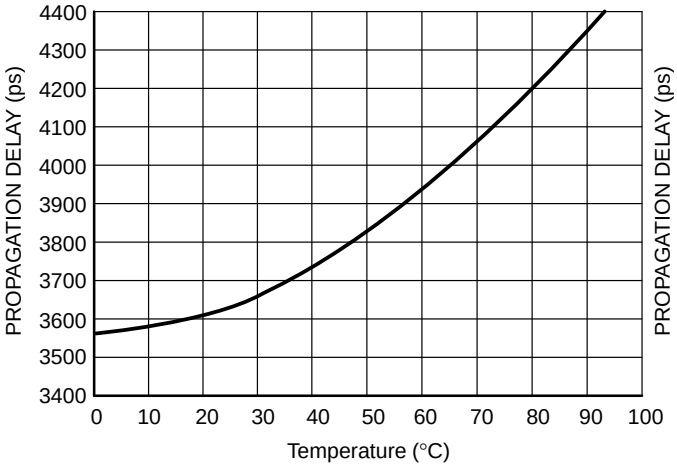


Figure 7. Delay vs. Temperature (Max. Delay).

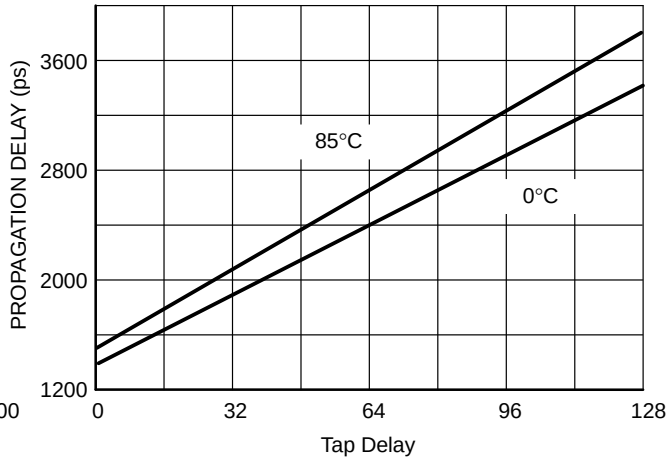


Figure 8. 100E195 Temperature Effects on Delay.

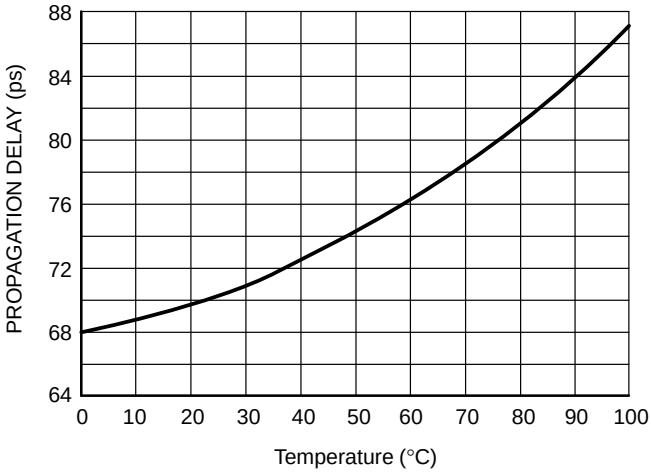


Figure 9. Delay vs. Temperature (Per Gate).

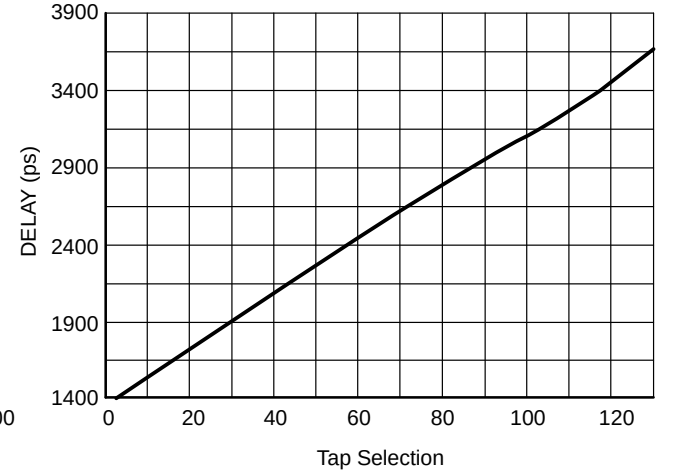


Figure 10. E195 Delay Linearity.

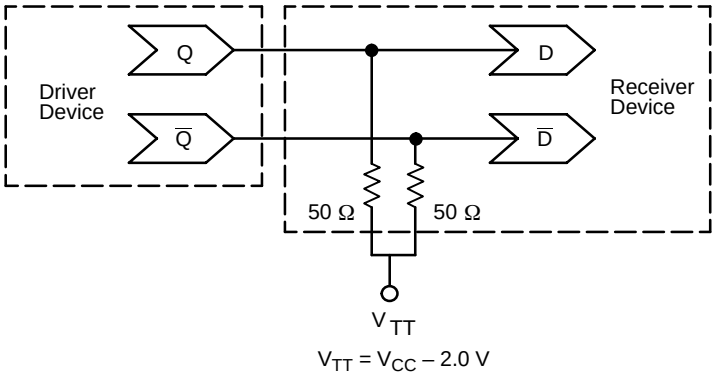


Figure 11. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

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PLCC–28
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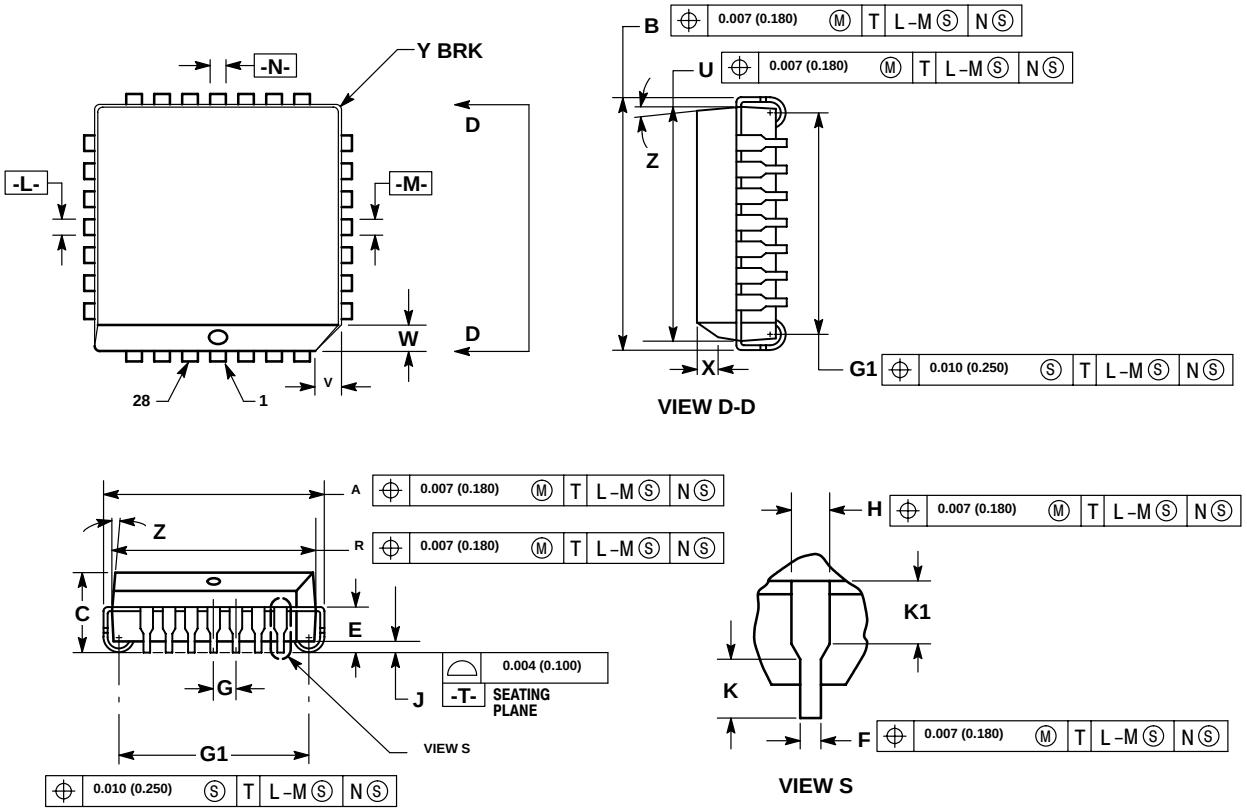
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

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