MIC2185

Low Voltage Synchronous Boost PWM Control IC

Final Information

General Description

Micrel's MIC2185 is a high efficiency synchronous boost PWM control IC. With its wide input voltage range of 2.9V to 14V, the MIC2185 can be used to efficiently boost voltages in 1- or 2-cell Li Ion battery powered applications, as well as fixed 3.3V and 5V systems. Its powerful 5Ω output drivers allow the MIC2185 to supply large output currents with the selection of the proper external MOSFETs.

With it's fixed frequency PWM architecture, and easily synchronized drive, the MIC2185 is ideal for noise-sensitive telecommunications applications. The nominal 400kHz operating frequency of the MIC2185 can be divided by two, allowing the device to be externally synchronized to frequencies below 400kHz.

The MIC2185 also features a low current shutdown mode and a programmable undervoltage lockout. A skipped pulse mode of operation can be manually set to achieve higher efficiencies at light load conditions.

The MIC2185 is available in a 16 pin SOIC package and 16 pin QSOP package with an ambient temperature operating range from –40°C to 85°C.

Features

- Input voltage range: 2.9V to 14V
- 95% efficiency
- Oscillator frequency of 200kHz/400kHz
- Frequency sync to 600kHz
- 0.5µA shutdown current
- Two 5Ω output drivers
- Front edge blanking
- PWM Current Mode Control
- Cycle-by-Cycle current limiting
- Frequency foldback protection
- Adjustable under-voltage lockout
- Precision 1.245V reference output
- 16 pin SOIC narrow body package and 16 pin QSOP package

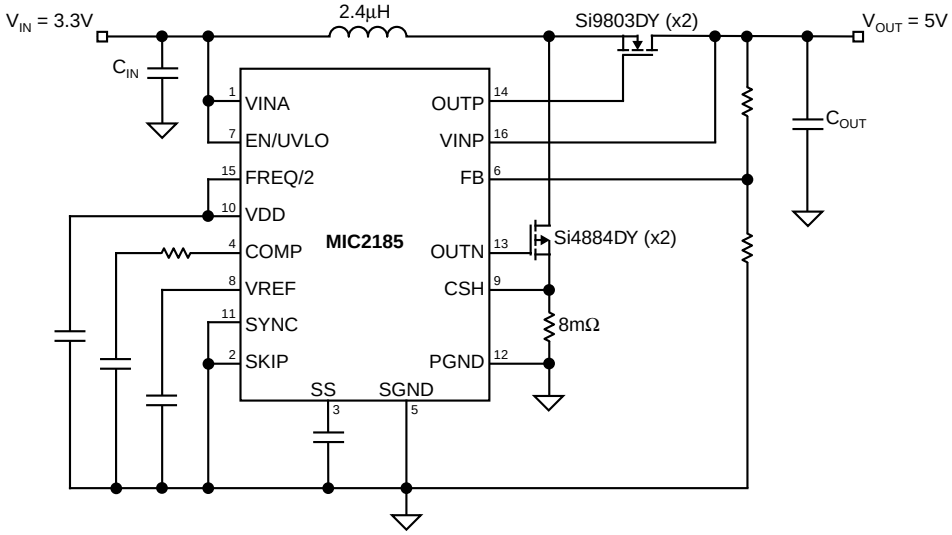
Applications

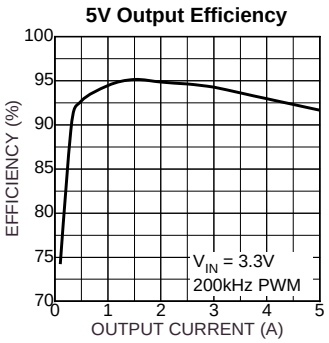
- 3.3V to 5V conversion in telecom systems
- Satellite Phones
- Cable Modems
- 1-and 2-cell Li Ion battery operated equipment

Ordering Information

Part Number	Frequency	Voltage	Junction Temp. Range	Package
MIC2185BM	200/400kHz	Adj	–40°C to +125°C	16-lead SOP
MIC2185BQS	200/400kHz	Adj	–40°C to +125°C	16-lead QSOP

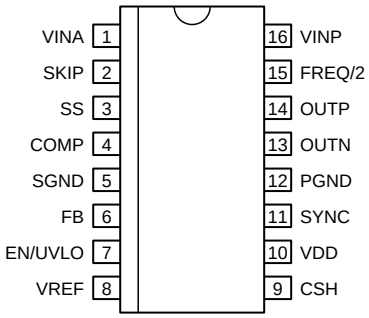
Typical Application





Adjustable Output Synchronous Boost Converter

Pin Configuration



16-pin Narrow Body SOP (M)
16-pin QSOP (QS)

Pin Description

Pin Number	Pin Name	Pin Function
1	VINA	Input voltage to control circuitry (2.9V to 14V).
2	SKIP	Skip (Input): Regulator operates in PWM mode (no pulse skipping) when pin is pulled low, and skip mode when raised to VDD. There is no automatic switching between PWM and skip mode available on this device.
3	SS	Soft Start (External Component) : Reduces the inrush current and delays and slows the output voltage rise time. A 5µA current source will charge the capacitor up to VDD.
4	COMP	Compensation (Output): Internal error amplifier output. Connect to a capacitor or series RC network to compensate the regulator's control loop.
5	SGND	Small Signal Ground (Return) : Must be routed separately from other grounds to the (–) terminal of C_{OUT}.
6	FB	Feedback (Input) : Regulates FB to 1.245V.
7	EN/UVLO	Enable/Undervoltaqe Lockout (Input): A low level on this pin will power down the device, reducing the quiescent current to under 0.5µA. This pin has two separate thresholds, below 1.5V (typical) the output switching is disabled, and below 0.9V (typical) the device is forced into a complete micropower shutdown. The 1.5V threshold functions as an accurate undervoltage lockout (UVLO) with 140mV hysteresis.
8	VREF	Voltage Reference (Output) : The 1.245V reference is available on this pin. A 0.1µF capacitor should be connected form this pin to SGnd.
9	CSH	Current Sense (Input) : The (+) input to the current limit comparator. A built in offset of 100mV (typical) between CSH and SGnd in conjunction with the current sense resistor sets the current limit threshold level. This is also the (+) input to the current amplifier.
10	VDD	3V Internal Linear-Regulator (Output) : VDD is also the supply voltage bus for the chip. Bypass to SGND with 1µF. Maximum source current is 0.5mA.
11	SYNC	Frequency Synchronization (Input): Connect an external clock signal to synchronize the oscillator. Leading edge of signal above 1.4V (typical) starts switching cycle. Connect to SGND if not used.
12	PGND	MOSFET Driver Power Ground (Return) : Connects bottom of current sense resistor and the (–) terminal of C_{IN}.
13	OUTN	N-Channel Drive (Output) : High current drive for n-channel MOSFET. Voltage swing is from ground to $V_{IN}P$. On-resistance is typically 5Ω.
14	OUTP	P-Channel Drive (Output) : High current drive for the synchronous p-channel MOSFET. Voltage swing is from ground to $V_{IN}P$. On-resistance is typically 5Ω.
15	FREQ/2	Frequency Divider (Input) : When this pin is low, the oscillator frequency is 400KHz. When this pin is raised to VDD, the oscillator frequency is 200KHz.
16	VINP	Gate Drive Voltage (Input) : This is the power input to the gate drive circuitry (2.9V to 14V). This pin is typically connected to the output voltage to enhance gate drive.

Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{IN}A$, $V_{IN}P$) 15V
Digital Supply Voltage (V_{DD}) 7V
Skip Pin Voltage (V_{SKIP}) ..... –0.3V to 7V
Comp Pin Voltage (V_{COMP}) ..... –0.3V to 3V
Feedback Pin Voltage (V_{FB}) ..... –0.3V to 3V
Enable Pin Voltage ($V_{EN/UVLO}$) ..... –0.3V to 15V
Current Sense Voltage (V_{CSH}) ..... –0.3V to 1V
Sync Pin Voltage (V_{SYNC}) ..... –0.3V to 7V
Freq/2 Pin Voltage ($V_{FREQ/2}$) ..... –0.3V to 7V
Power Dissipation (P_D)
16 lead SOP ..... 400mW @ T_A = 85°C
16 lead QSOP ..... 245mW@ T_A = 85°C
Ambient Storage Temp ..... –65°C to +150°C

Operating Ratings (Note 2)

Supply Voltage ($V_{IN}A$, $V_{IN}P$) ..... +2.9V to +14V
Operating Ambient Temperature ..... $–40°C \le T_A \le +85°C$
Junction Temperature ..... $–40°C \le T_J \le +125°C$
PackageThermal Resistance
θ_{JA} 16-lead SOP ..... 100°C/W
θ_{JA} 16-lead QSOP ..... 163°C/W
ESD Rating, **Note 3**

Electrical Characteristics

$V_{IN}A$= 5V, VinP= V_{OUT}=12V, $V_{EN/UVLO}$ = 5V, V_{SKIP} = 0V, $V_{FREQ/2}$ = 0V, V_{CSH} = 0V, T_J = 25°C, unless otherwise specified. **Bold** values indicate $–40°C < T_J < +125°C$.

Parameter	Condition	Min	Typ	Max	Units
Regulation					
Feedback Voltage Reference	(±1%)	1.233	1.245	1.258	V
	(±2%)	**1.220**		**1.270**	V
	$3V \le V_{IN}A \le 9V$; $0mV \le CSH \le 75mV$; (±3%)	1.208	1.245	1.282	V
Feedback Bias Current			50		nA
Output Voltage Line Regulation	$3V \le V_{IN}A \le 9V$		+0.08		% / V
Output Voltage Load Regulation	$0mV \le CSH \le 75mV$		–1.2		%
Input & V_{DD} Supply					
$V_{IN}A$ Input Current, PWM mode	V_{SKIP} = 0V		0.8		mA
$V_{IN}P$ Input Current, PWM mode	V_{SKIP} = 0V (excluding external MOSFET gate current)		3.8		mA
$V_{IN}A$ Input Current, SKIP mode	V_{SKIP} = 5V		0.6		mA
Shutdown Quiescent Current	$V_{EN/UVLO}$ = 0V; (I_{VINA} + I_{VINP})		0.5		µA
Digital Supply Voltage (VDD)	I_L = 0	2.8	3.0	3.2	V
Digital Supply Load Regulation	I_L = 0 to 0.5mA		0.03		V
Undervoltage Lockout	V_{DD} upper threshold (turn on threshold)	2.9	2.75		V
	V_{DD} lower threshold (turn off threshold)		2.65		V
Reference Output (V_{REF})					
Reference Voltage	(±1.5%)	1.226	1.245	1.264	V
	(±2.5%)	**1.213**		**1.276**	V
Reference Voltage Line Regulation	5V < VinA < 9V		2		mV
Reference Voltage Load Regulation	$0 < I_{REF} < 100µA$		1		mV
Enable/UVLO					
Enable Input Threshold		0.6	0.9	1.2	V
UVLO Threshold		1.4	1.5	1.6	V
UVLO Hysteresis			140		mV
Enable Input Current	$V_{EN/UVLO}$ = 5V		0.2	5	µA

Parameter	Condition	Min	Typ	Max	Unit
Soft Start					
Soft Start Current			5		µA
Current Limit					
Current Limit Threshold Voltage	Voltage on CSH to trip current limit		100		mV
Error Amplifier					
Error Amplifier Gain			20		V/V
Current Amplifier					
Current Amplifier Gain			3.7		V/V
SKIP Input					
SKIP Threshold		0.6	1.4	2.2	V
SKIP Input Current	V_{SKIP} = 3V		0.1	5	µA
Oscillator Section					
Oscillator Frequency (f_S)		360	400	440	kHz
Maximum Duty Cycle	V_{FB} = 1.0V		85		%
Minimum On Time	V_{FB} = 1.5V		180		ns
FREQ/2 frequency (f_S)	$V_{FREQ/2}$=3V	170	200	230	
Frequency Foldback Threshold	Measured at FB pin		0.3		V
Frequency Foldback Frequency	$V_{FREQ/2}$=0V		90		kHz
SYNC Threshold Level		0.6	1.4	2.2	V
SYNC Input Current			0.1	5	µA
SYNC Minimum Pulse Width		200			ns
SYNC Capture Range	**Note 4**	f_O+15 %		600	kHz
Gate Drivers (OUTN and OUTP)					
Rise/Fall Time	C_L = 3300pF		50		ns
Driver Non-overlap Time	$V_{IN}P$ = 12V		70		ns
	$V_{IN}P$ = 5V		90		ns
Output Driver Impedance	Source; $V_{IN}P$ = 12V		4	**8**	Ω
	Sink; $V_{IN}P$ = 12V		3	**7**	Ω
	Source; $V_{IN}P$ = 5V		5	**11**	Ω
	Sink; $V_{IN}P$ = 5V		5	**11**	Ω

Note 1. Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(max)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A.

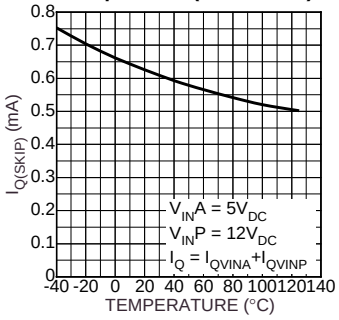
Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended.

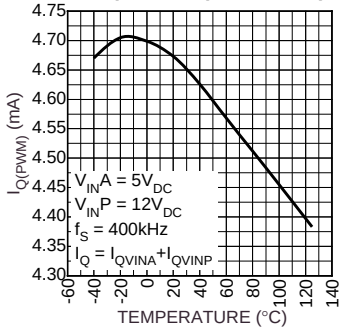
Note 4. See application information for limitations on maximum operating frequency.

Typical Characteristics

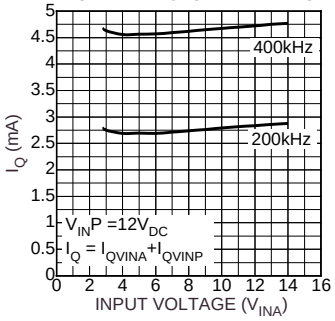
Quiescent Current vs. Temperature (SKIP Mode)



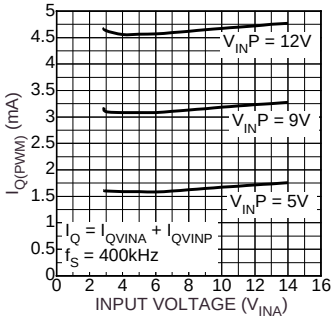
Quiescent Current vs. Temperature (PWM Mode)



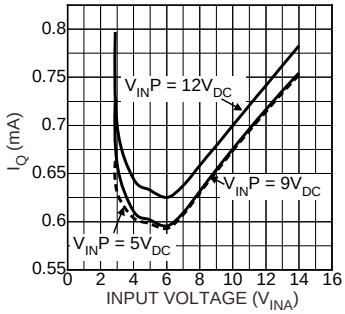
Quiescent Current vs. Input Voltage(PWM Mode)



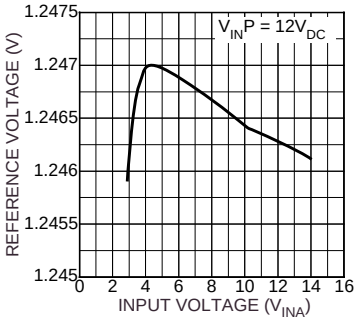
Quiescent Current vs. Input Voltage (PWM Mode)



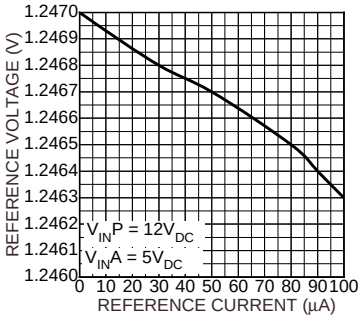
Quiescent Current vs. Input Voltage (SKIP Mode)



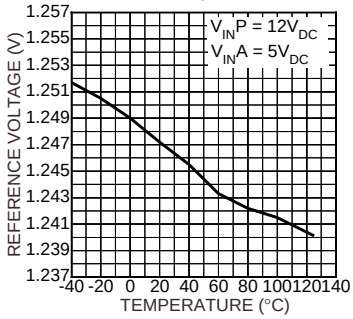
Reference Voltage vs. Input Voltage



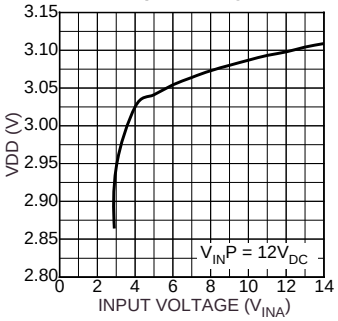
Reference Voltage vs. Reference Current



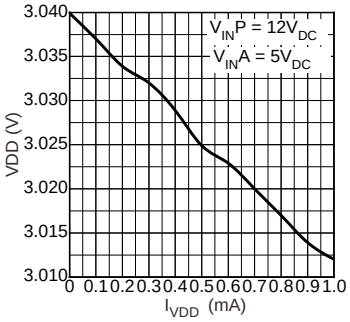
Reference Voltage vs. Temperature



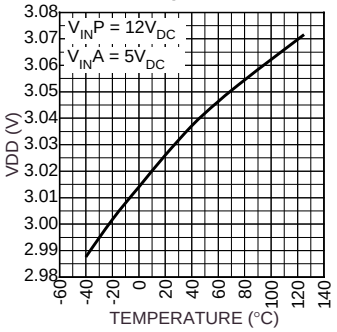
VDD vs. Input Voltage



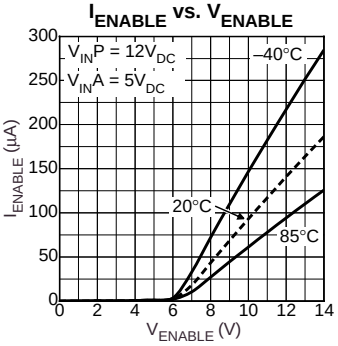
VDD vs. Load Current



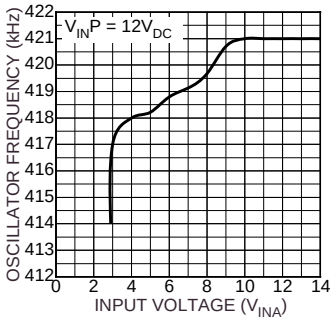
VDD vs. Temperature



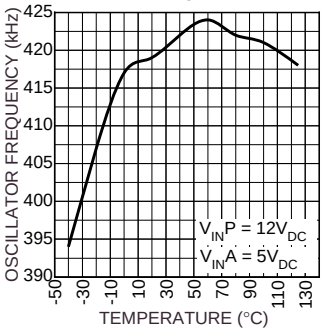
I_{ENABLE} vs. V_{ENABLE}



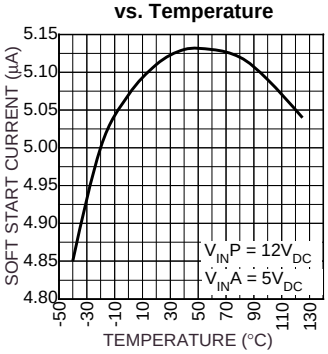
Oscillator Frequency vs. Input Voltage



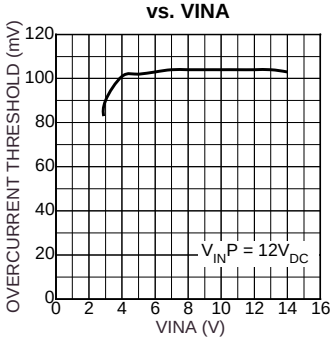
Oscillator Frequency vs. Temperature



Soft Start Current vs. Temperature



Overcurrent Threshold vs. VINA



Functional Diagram

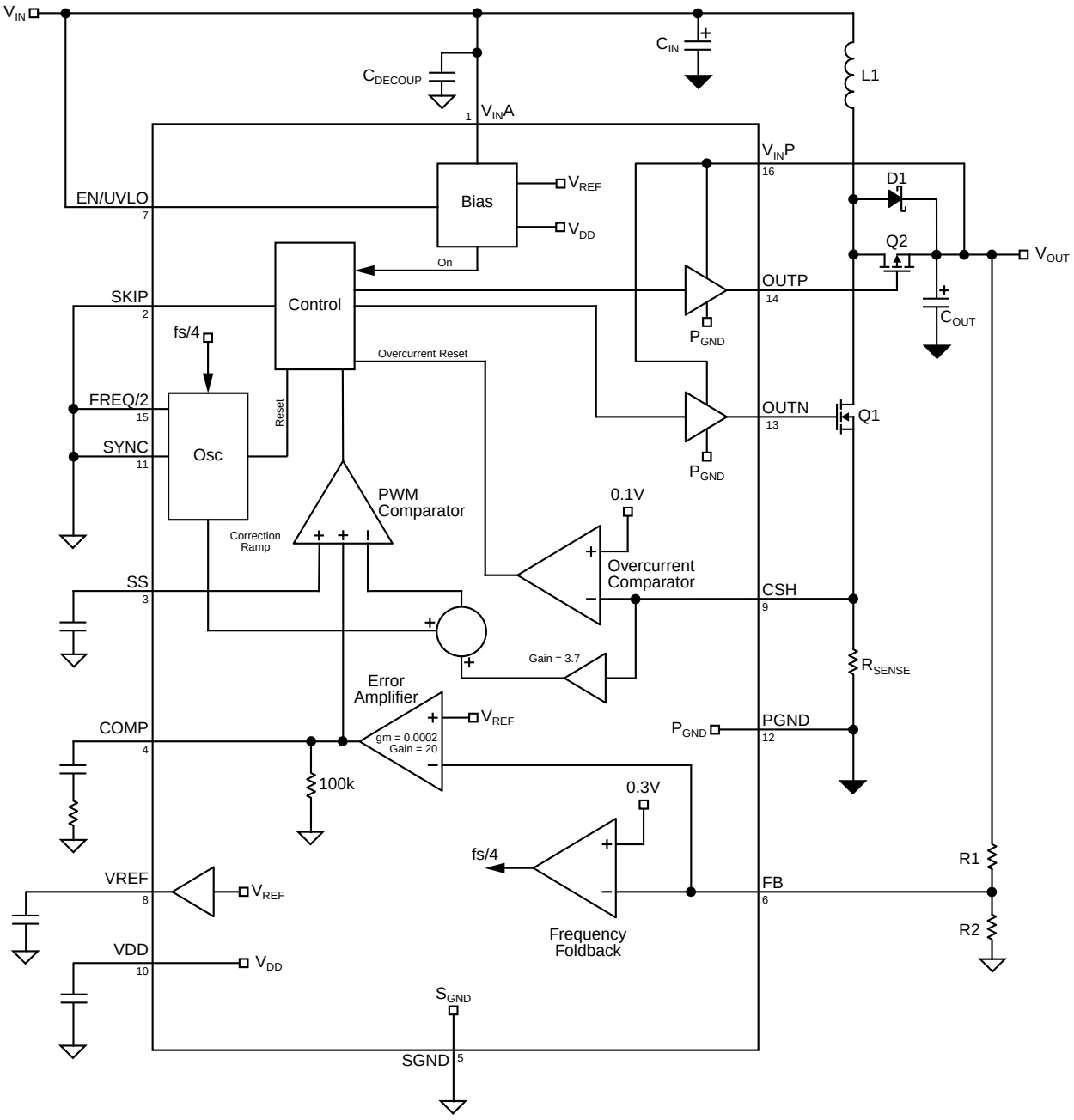


Figure 1. MIC2185 PWM Mode Block Diagram

Functional Description

The MIC2185 is a BiCMOS, switched mode, synchronous boost (step up) control IC. The synchronous switched, high side P-channel MOSFET, Q2, placed in parallel with the output diode, D1, improves the efficiency of the boost converter. The lower voltage drop across the MOSFET reduces power dissipation and increases efficiency. Current mode control is used to achieve superior transient line and load regulation. An internal corrective ramp provides slope compensation for stable operation above a 50% duty cycle. The controller is optimized for high efficiency, high performance DC-DC converter applications.

Figure 1 is a block diagram of the MIC2185 configured as a PWM synchronous boost converter. The switching cycle starts when OutN goes high and turns on the low side, N-channel MOSFET, Q1. The Vgs of the MOSFET is equal to VinP. This forces current to ramp up in the inductor. The inductor current flows through the current sense resistor, Rsense. The voltage across the resistor is amplified and combined with an internal ramp for stability. This signal is compared with the comp output signal of the error amplifier. When the current signal equals the error voltage signal, the low side MOSFET is turned off. The inductor current then flows through the diode, D1, to the output. A delay between the turn-off of the low side MOSFET and the turn-on of the high side MOSFET prevents both MOSFETs from being on at the same time, which would short the output to ground. At the end of the non-overlap time, OutP pulls the gate of the MOSFET to ground, turning on the high side, P-channel

MOSFET, Q2. Current flows through the MOSFET because its voltage drop is less than diode D1. The MOSFET remains on until the end of the switching cycle. There is another non-overlap time delay between the turn-off of the high side MOSFET and the turn-on of the low side MOSFET at the beginning of the next switching cycle.

The description of the MIC2185 controller is broken down into 6 basic functions.

- Control Loop
  - PWM Operation
  - SKIP Mode Operation
- Current Limit
- MOSFET gate drive
- Reference, Enable & UVLO
- Oscillator & Sync
- Soft Start

Control Loop

PWM and SKIP modes of operation

The MIC2185 can operate in either PWM (pulse width modulated) or skip mode. The efficiency of the boost converter can be improved at lower output loads by manually selecting the skip mode of operation. The potential disadvantage of skip mode is the variable switching frequency that accompanies this mode of operation. The occurrence of switching pulses depends on component values as well as line and load conditions. PWM mode is the best choice of operation at higher output loads. In skip mode, current through the inductor can settle to zero, causing voltage ringing across the inductor. PWM mode has the advantages of lower output ripple voltage and higher efficiencies at higher output loads. Another advantage of the synchronous PWM mode of operation is that the inductor current is always continuous, even at

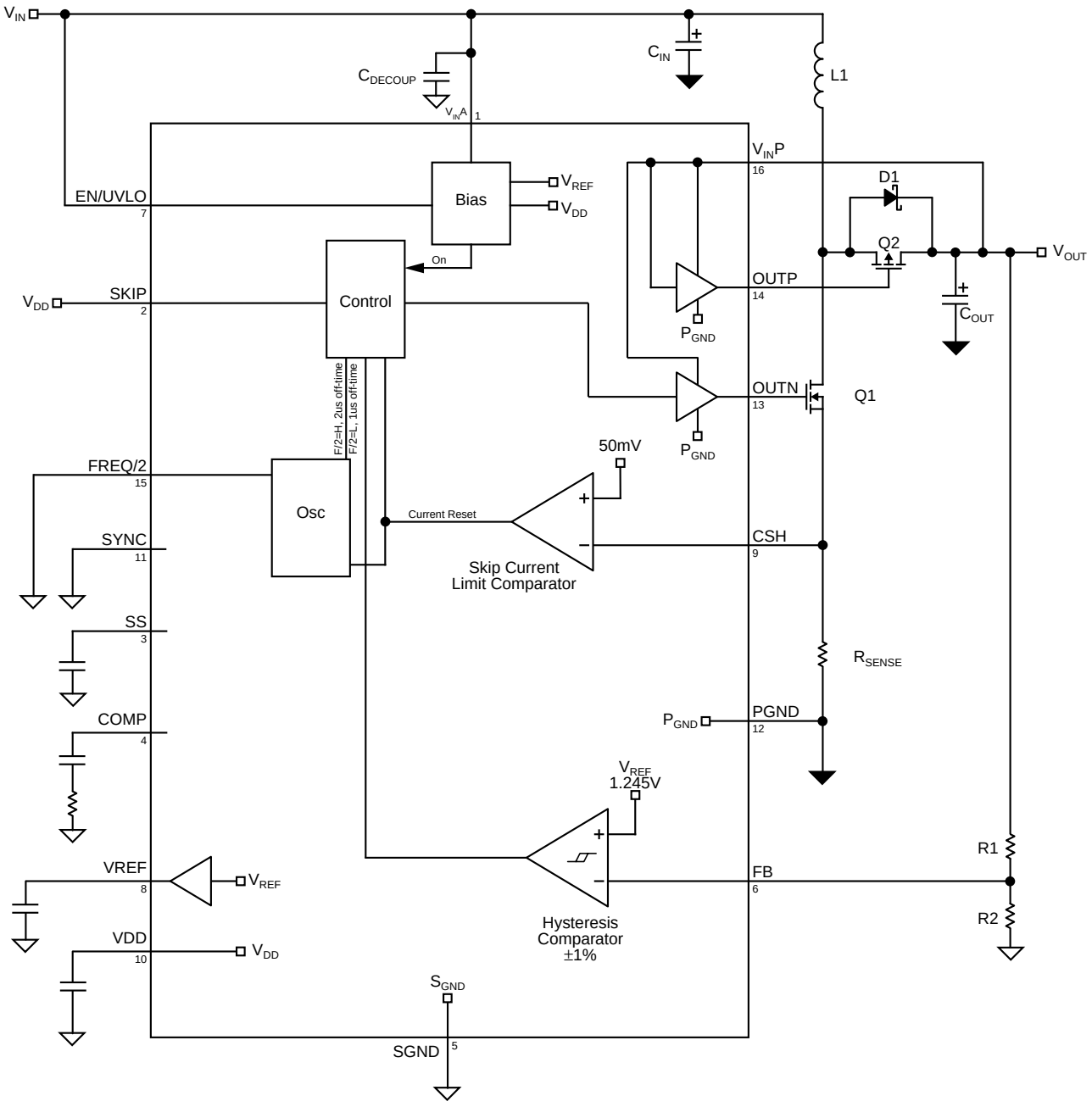


Figure 2. MIC2185 Skip Mode Block Diagram

zero output current. This reduces parasitic ringing that occurs during the discontinuous mode of operation found in lightly loaded, non-synchronous boost converters. Pulling the SKIP pin (pin 2) low will force the controller to operate in PWM mode for all load conditions. Pulling the SKIP pin high will force the controller to operate in SKIP mode.

Skip Mode Operation

This control method is used to improve efficiency at low output loads. A block diagram of the MIC2185 skip mode is shown in Figure 2. The power drawn by the MIC2185 control IC is $(I_{VINA} \cdot V_{VINA}) + (I_{VINP} \cdot V_{VINP})$. The power dissipated by the IC can be a significant portion of the total output power during periods of low output current, which lowers the efficiency of the power supply. In skip mode the MIC2185 lowers the IC supply current by disabling the high side drive and running at lower than the PWM switching frequency. It also turns off portions of the control and drive circuitry when the IC is not switching. The disadvantage of this method is greater output ripple and variable switching frequency. The Soft Start and Sync pins have no effect when operating in skip mode.

In skip mode, switching starts when the feedback voltage drops below the lower threshold level of the hysteresis comparator. The OutN pin goes high, turning on the N-channel MOSFET, Q1. Current ramps up in the inductor until either the SKIP mode current limit comparator or the hysteretic voltage comparator turns off Q1's gate drive. If the feedback voltage exceeds the upper hysteretic threshold, Q1's gate drive is terminated. Or, if the voltage at the CSH pin exceeds the skip mode current limit threshold, it terminates the gate drive for that switching cycle. The gate drive remains off for a constant period at the end of each switching cycle. This off time period is typically 1us when the F/2 pin is low and 2us when the F/2 pin is high. Figure 3 shows some typical switching waveforms in SKIP mode.

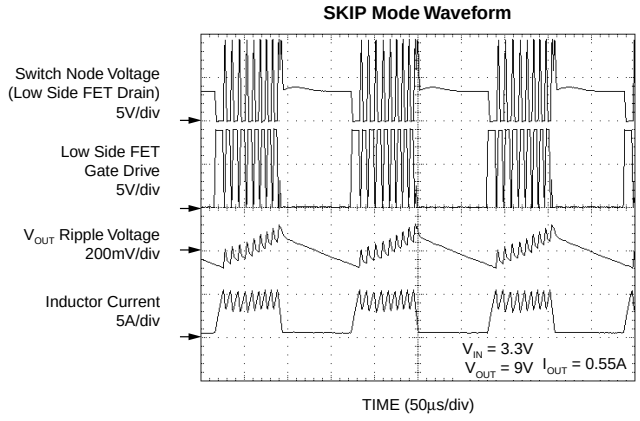


Figure 3. SKIP mode waveforms

The skip mode current threshold limits the peak inductor current per cycle. Depending on the input, output and circuit parameters, many switching cycles can occur before the feedback voltage exceeds the upper hysteretic threshold. Once the voltage on the feedback pin exceeds the upper hysteretic threshold the gate drive is disabled. The output load discharges the output capacitance causing Vout to decrease until the feedback voltage drops below the lower threshold voltage limit. The switching converter then turns the gate drive back on. While the gate drive is disabled, the MIC2185 draws less IC supply current then while it is switching, thereby improving efficiency at low output loads.

Figure 4 shows the improvement in efficiency that SKIP mode makes when at lower output currents.

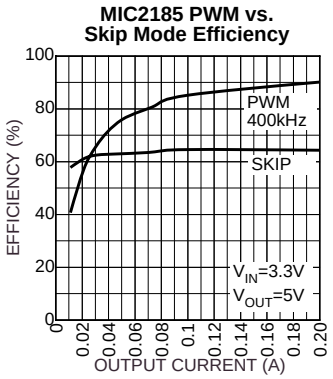


Figure 4.

The maximum peak inductor current depends on the skip current limit threshold and the value of the current sense resistor, R_{SENSE}. For a typical 50mV current limit threshold in skip mode, the peak inductor current is:

$$I_{INDUCTOR\_pk} = \frac{50mV}{R_{SENSE}}$$

The maximum output current in skip mode depends on the input conditions, output conditions and circuit component values. Assuming a discontinuous mode where the inductor current starts from zero at each cycle, the maximum output current is calculated below:

$$I_{O(max)} = \frac{2.5 \times 10^{-3} \times L \times fs}{2 \times R_{SENSE}^{2} \times \left(V_O - \left(\eta \times V_{IN}\right)\right)}$$

where: $I_{O(max)}$ is the maximum output current

V_O is the output voltage

V_{IN} is the input voltage

L is the value of the boost inductor

f_S is the switching frequency

η is the efficiency of the boost converter

R_{SENSE} is the value of the current sense resistor

$2.5 \cdot 10^{-3}$ is a constant based on the skip mode current threshold $(50mV)^2$

PWM Operation

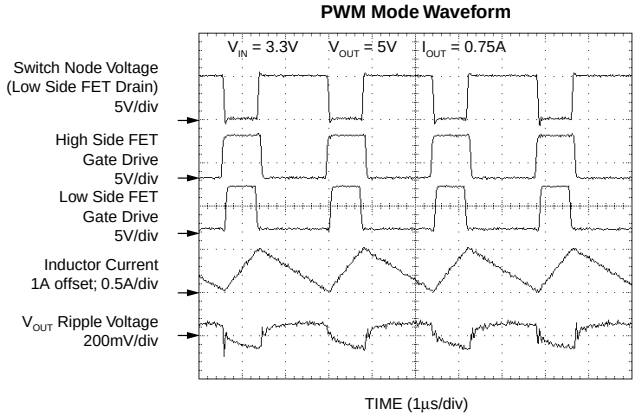


Figure 5 - PWM mode waveforms

Figure 5 shows typical waveforms for PWM mode of operation. The gate drive signal turns on the external low side MOSFET, Q1, allowing the inductor current to ramp up. When the low side MOSFET turns off and the high side MOSFET, Q2, turns on, current flowing in the inductor forces the MOSFET drain voltage to rise until the is clamped at approximately the output voltage. The MIC2185 uses current mode control to improve output regulation and simplify compensation of the control loop. Current mode control senses both the output voltage (outer loop) and the inductor current (inner loop). It uses the inductor current and output voltage to determine the duty cycle (D) of the buck converter. Sampling the inductor current effectively removes the inductor from the control loop, which simplifies compensation. A simplified current mode control diagram is shown in figure 6.

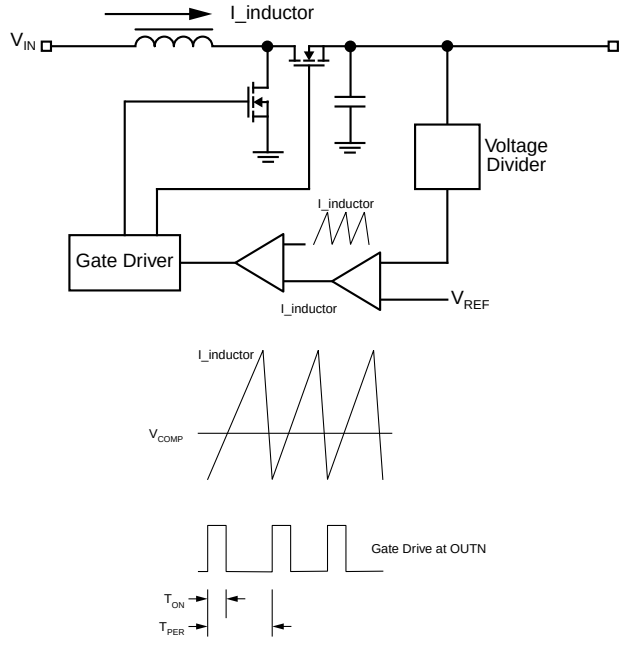


Figure 6. PWM Control Loop

A block diagram of the MIC2185 PWM current mode control loop is shown in Figure 1. The inductor current is sensed by measuring the voltage across a resistor, Rsense. The current sense amplifier buffers and amplifies this signal. A ramp is added to this signal to provide slope compensation, which is required in current mode control to prevent unstable operation at duty cycles greater than 50%.

A transconductance amplifier is used as an error amplifier, which compares an attenuated output voltage with a reference voltage. The output of the error amplifier is compared to the current sense waveform in the PWM block. When the current signal rises above the error voltage, the comparator turns off the low side drive. The error signal is brought out to the COMP pin (pin 4) allowing the use of external components to stabilize the voltage loop.

Current Sensing and Overcurrent Protection

The inductor current is sensed during the switch on time by a current sense resistor located between the source of the MOSFET, Q1 and ground (R_{SENSE} in Figure 1). Exceeding the current limit threshold will immediately terminate the gate drive of the N-channel MOSFET. This forces the Q1 to operate at a reduced duty cycle, which reduces the output voltage. **In a boost converter, the overcurrent limit will not protect the power supply or load during a severe overcurrent condition or short circuit condition.** If the output is short-circuited to ground, current will flow from the input, through the inductor and output diode,D1, to ground. Only the impedance of the source and components limits the current.

The minimum input voltage, maximum output power and the minimum value of the current limit threshold determine the value of the current sense resistor. The two switch, synchronous operation of the MIC2185 forces the converter to always operate in the continuous mode because current can flow both ways through the high side P-channel MOSFET. The equations below will help to determine the current sense resistor value.

Maximum Peak Current

The peak inductor current is equal to the average inductor current plus one half of the peak to peak inductor current.

The peak inductor current is:

$$I_{IND(pk)} = I_{IND(ave)} + \frac{1}{2} \times I_{IND(pp)}$$

$$I_{IND(pk)} = \frac{V_O \times I_O}{V_{IN} \times \eta} + \frac{V_L \times \left(V_O - \left(V_{IN} \times \eta\right)\right)}{2 \times V_O \times fs \times L}$$

where:

I_O is the maximum output current

V_O is the output voltage

V_{IN} is the minimum input voltage

L is the value of the boost inductor

f_S is the switching frequency

η is the efficiency of the boost converter

V_L is the voltage across the inductor

V_L may be approximated as V_{IN} for higher input voltage. However, the voltage drop across the inductor winding resistance and low side MOSFET on-resistance must be accounted for at the lower input voltages that the MIC2185 can operate at.

$$V_L = V_{IN} - \frac{V_O \times I_O}{V_{IN} \times \eta} \times \left(R_{WINDING} + R_{DS(ON)}\right)$$

where:

$R_{WINDING}$ is the winding resistance of the inductor

$R_{DS(ON)}$ is the on resistance of the low side switching MOSFET

The maximum value of current sense resistor is:

$$R_{SENSE} = \frac{V_{SENSE}}{I_{IND(pk)}}$$

where:

V_{SENSE} is the minimum current sense threshold of the CSH pin

The current sense pin, CSH, is noise sensitive due to the low signal level. The current sense voltage measurement is referenced to the signal ground pin of the MIC2185. The current sense resistor ground should be located close to the IC ground. Make sure there are no high currents flowing in this trace. The PCB trace between the high side of the current sense resistor and the CHS pin should also be short and routed close to the ground connection. The input to the internal current sense amplifier has a 30nS dead time at the beginning of each switching cycle. This dead time prevents leading edge current spikes from prematurely terminating the switching cycle. A small RC filter between the current sense pin and current sense resistor may help to attenuate larger switching spikes or high frequency switching noise. Adding the filter slows down the current sense signal, which has the effect of slightly raising the overcurrent limit threshold.

MOSFET Gate Drive

The MIC2185 synchronous boost converter drives both a high side and low side MOSFET. The low side drive, OUTN, drives an n-channel MOSFET. The high-side drive, OUTP, is designed to switch a p-channel MOSFET (the p-channel MOSFET doesn't require a bootstrap circuit which would be needed to drive an n-channel MOSFET). The $V_{IN}P$ pin must be connected to the output, which provides power to drive the high and low side MOSFETs. In skip mode, the high side MOSFET is disabled by forcing the OUTP pin to be high (equal to V_{OUT}).

MOSFET Selection

In a boost converter, the V_{DS} of the MOSFET, Q1, is approximately equal to the output voltage. The maximum Vds rating of the MOSFET must be high enough to allow for ringing and spikes. The MIC2185 input voltage range is 2.9V to 14V. MOSFETs with 20V and 30V V_{DS} ratings are ideal for use with this part.

The n-channel gate drive voltage is supplied by the OUTN output. At startup in a boost converter, the output voltage equals the input voltage. The V_{GS} threshold voltage of the n-channel MOSFET must be low enough to operate at the minimum input voltage to guarantee the boost converter will start up. The p-channel MOSFET must have a minimum threshold voltage equal to or lower than the output voltage. Five volt threshold (logic level) MOSFETs are recommended for the p-channel MOSFET. Ringing in the gate drive signal may cause MOSFETs with lower gate thresholds to erroneously turn on.

There is a limit to the maximum amount of gate charge the MIC2185 will drive. Higher gate charge will slow down the turn-on and turn-off times of the MOSFETs. The MOSFET's must be able to completely turn on and off within the driver non-overlap time or shoot-through will occur.

MOSFET gate charge is also limited by power dissipation in the MIC2186. The power dissipated by the gate drive circuitry is calculated below:

$$P_{GATE\_DRIVE} = Q_{GATE} \cdot V_{IN}P \cdot f_S$$

where: Q_{GATE} is the total gate charge of both of the external n- and p-channel MOSFETs.

The graph in Figure 7 shows the total gate charge which can be driven by the MIC2185 over the input voltage range, for different values of switching frequency.

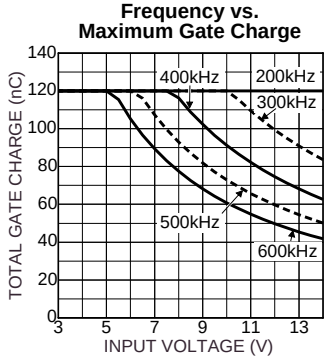


Figure 7 - MIC2185 Frequency vs. Max. Gate Charge

External Schottky Diode

An external boost diode in parallel with the high side MOSFET is used to keep the inductor current flow continuous during the non-overlap time when both MOSFETs are turned off. Although the average current through this diode is small, the diode must be able to handle currents equal to the peak inductor current. This peak current is calculated in the Current Limit section of this specification

The reverse voltage requirement of the diode is:

$$V_{DIODE\_RRM} = V_{OUT}$$

For the MIC2185, Schottky diodes with a 30V or 40V rating are recommended. Schottky diodes with lower reverse voltage ratings have higher reverse leakage current which will cause ringing and excessive power dissipation in the diode and low side MOSFET.

The external Schottky diode is not necessary for circuit operation since the high side MOSFET contains a parasitic body diode. However, the body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The lower forward voltage drop of the Schottky diode both prevents the parasitic diode from turning on and improves efficiency. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing than the MOSFET's parasitic diode. Depending on the circuit components and operating conditions, an external Schottky diode will improve the converter efficiency by $^1/_2$% to 1%.

Reference, Enable and UVLO Circuits

The output drivers are enabled when the following conditions are satisfied:

- The VDD voltage (pin 10) is greater than its undervoltage threshold.
- The voltage on the Enable pin is greater than the Enable /UVLO threshold.

The internal bias circuitry generates a 1.245V bandgap reference for the voltage error amplifier and a 3V V_{DD} voltage for the internal supply bus. The reference voltage in the MIC2185 is buffered and brought out to pin 8. The VREF pin must be bypassed to GND (pin 4) with a 0.1µF capacitor. The VDD pin must be decoupled to ground with a 1µF ceramic capacitor.

The Enable pin (pin 7) has two threshold levels, allowing the MIC2185 to shut down in a micro-current mode, or turn off output switching in standby mode. Below 0.9V (typical), the device is forced into a low-power shutdown. If the enable pin is between 0.9V and 1.5V (typical) the output gate drive is disabled but the internal circuitry is powered on and the soft start pin voltage is forced low. There is typically 140mV of hysteresis below the 1.5V threshold to insure the part does not oscillate on and off due to ripple voltage on the input. Raising the Enable voltage above the UVLO threshold of 1.5V enables the output drivers and allows the soft start capacitor to charge. The Enable pin may be pulled up to V_{IN}A.

Oscillator & Sync

The internal oscillator is self-contained and requires no external components. The f/2 pin allows the user to select from two switching frequencies. A low level sets the oscillator frequency to 400kHz and a high level sets the oscillator frequency to 200kHz. The maximum duty cycle for both frequencies is typically 85%. The minimum pulse width increases but does not double when the frequency is changed from 400kHz to 200kHz. This means the minimum duty cycle is slightly lower at 200kHz. This may be important as the input voltage approaches the output voltage. At lower duty cycles, the input voltage can be closer to the output voltage without the output rising out of regulation.

A frequency foldback mode is enabled if the voltage on the Feedback pin (pin 6) is less than 0.3V. In frequency foldback the oscillator frequency is reduced by approximately a factor of 4. For the 400kHz setting, the oscillator runs at 100khz in frequency foldback. For a 200kHz setting the oscillator runs at approximately 50kHz.

The SYNC input (pin 11) allows the MIC2185 to synchronize with an external CMOS or TTL clock signal. The rising edge of the sync signal generates a reset signal in the oscillator, which turns off the high side gate drive output. The low side-drive then turns on, restarting the switching cycle. The sync signal is inhibited when the controller operates in skip mode or frequency foldback. The sync signal frequency must be greater than the maximum specified free running frequency of the MIC2185. If the synchronizing frequency is lower, double pulsing of the gate drive outputs will occur. When not used, the sync pin must be connected to ground.

Figure 8 shows the timing between the external sync signal, low side-drive and the high side drive when the f/2 pin is low. The delay between the rising edge of the sync signal and the turn on of the low side gate drive is typically 900ns when the f/2 pin is high and 600ns when the f/2 pin is low.

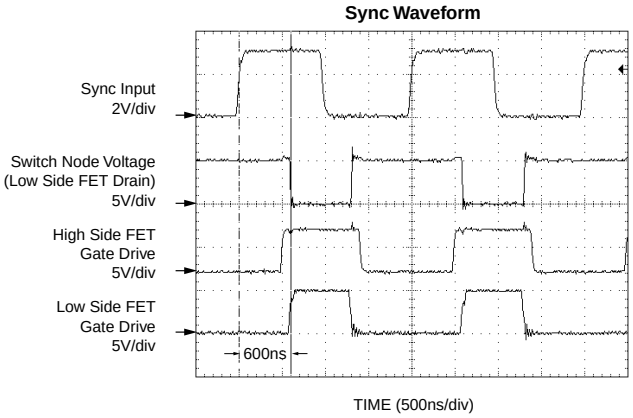


Figure 8. Sync Waveforms

The maximum recommended output switching frequency is 600kHz. Synchronizing to higher frequencies may be possible, however there are some concerns. As the switching frequency is increased, the switching period decreases. The minimum on time in the MIC2185 becomes a greater part of the total switching period. This may prevent proper operation as Vin approaches Vout and may also minimize the effectiveness of the current limit circuitry. The maximum duty cycle decreases as the sync frequency is increased. Figure 9 shows the relationship between the minimum and maximum duty cycle and frequency.

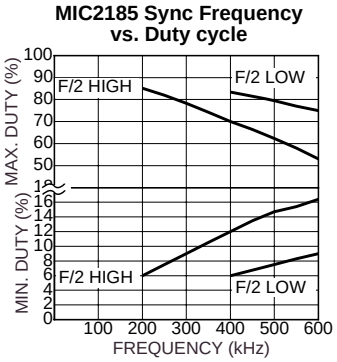


Figure 9

Table 1 summarizes the differences in the MIC2185 for the two different states of the f/2 pin.

F/2 pin Level	Switching Frequency (kHz)	Typical Max Duty cycle (%)	Typical Min. Duty cycle (%)	t_{OFF} in SKIP Mode
0	400	85	6	1µs
1	200	85	6	2µs

MIC2185 Table 1

Soft Start

Soft Start reduces the power supply input surge current at start up by limiting the output voltage rise time. Input surge current occurs when the boost converter charges up the output capacitance. Slowing the output rise time lowers the input surge current. Soft Start may also be used for power supply sequencing. The soft start cannot control the initial surge of current in a boost converter when V_{IN} is applied. This surge current is caused by the output capacitance charging up to the input voltage. The current flows from the input through the inductor and output diode to the output capacitors.

The soft start voltage is applied directly to the PWM comparator. A 5µA internal current source is used to charge up the soft start capacitor. Either of 2 UVLO conditions will pull the soft start capacitor low.

- When the V_{DD} voltage drops below its UVLO threshold
- When the Enable pin drops below the UVLO threshold

The part switches at a low duty cycle when the soft start pin voltage zero. As the soft start voltage rises from 0V to 0.7V, the duty cycle increases from the minimum duty cycle to the operating duty cycle. The oscillator runs at the foldback frequency until the feedback voltage rises above 0.3V. In a boost converter the output voltage is equal to the input voltage before the MIC2185 starts switching. If the ratio of Vout/Vin is low, the voltage on the feedback pin will already be greater than 0.3V and the converter begin switching at the selected operating frequency.

The risetime of the output is dependent on the soft start capacitor, output capacitance, input and output voltage and load current. The scope photo in Figure10 shows the output voltage and the soft start pin voltage at startup. The output voltage is initially at the input voltage less a diode drop. After the converter is enabled the output slowly rises due to the minimum duty cycle of the controller. As the soft start voltage increases, the output voltage rises in a controlled fashion until the output voltage reaches the regulated value.

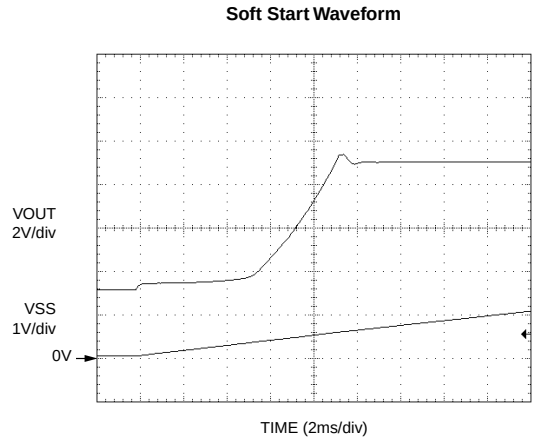


Figure 10 Soft Start

Voltage Setting Components

The MIC2185 requires two resistors to set the output voltage as shown in Figure 11

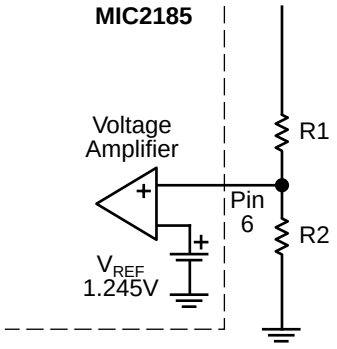


Figure 11

The output voltage is determined by the equation below.

$$V_O = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where:

V_{REF} for the MIC2185 is nominally 1.245V.

Lower values of resistance are preferred to prevent noise from apprearing on the V_{FB} pin. A typically recommended value for R1 is 10kΩ.

Decoupling Capacitor Selection

A 1µF decoupling capacitor is used to stabilize the internal regulator and minimize noise on the VDD pin. Placement of this capacitor is critical to the proper operation of the MIC2185. It must be next to the VDD and signal ground pins. The capacitor should be a good quality ceramic. Incorrect placement of the VDD decoupling capacitor will cause jitter and/or oscillations in the switching waveform as well as variations in the overcurrent limit.

A minimum 0.1µF ceramic capacitor is required to decouple the V_{IN} pin. The capacitor should be placed near the IC and connected directly between pin 10 (VDD) and pin 5 (SGND). A 0.1µF capacitor is required to decouple VREF. It should be located near the VREF pin.

Efficiency calculation and considerations

Efficiency is the ratio of output power to input power. The difference is dissipated as heat in the boost converter. The significant contributors at light output loads are:

- The V_{IN}A pin supply current.
- The V_{IN}P pin supply current which includes the current required to switch the external MOSFETs
- Core losses in the inductor

To maximize efficiency at light loads:

- Use a low gate charge MOSFET or use the smallest MOSFET, which is still adequate for the maximum output current.
- Allow the MIC2185 to run in skip mode at lower currents. If running in PWM mode, set the frequency to 200kHz.
- Use a ferrite material for the inductor core, which has less core loss than an MPP or iron power core.

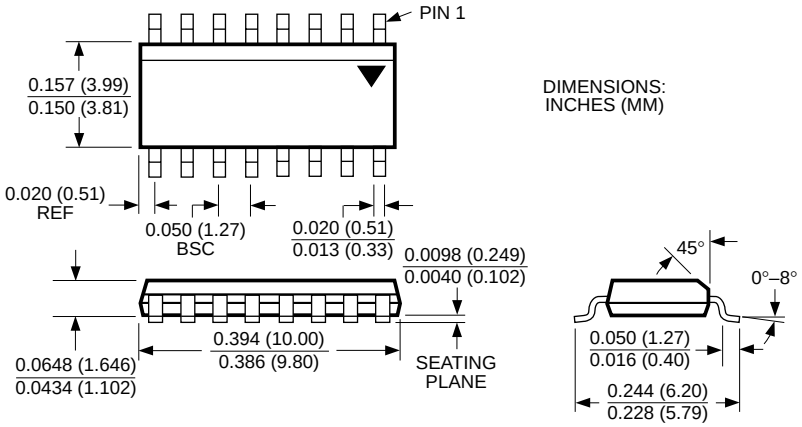
The significant contributors to power loss at higher output loads are (in approximate order of magnitude):

- Resistive on-time losses in both MOSFETs
- Switching transition losses in the low side MOSFET
- Inductor resistive losses
- Current sense resistor losses
- Output capacitor resistive losses (due to the capacitor's ESR)

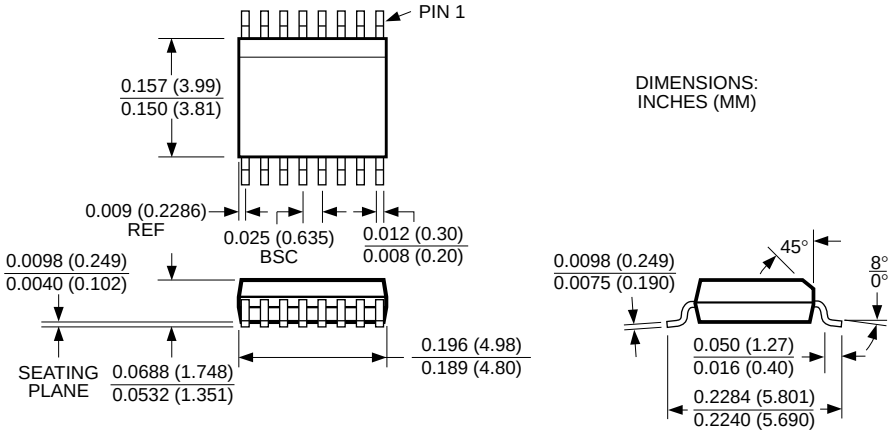
To minimize power loss under heavy loads:

- Use logic level, low on-resistance MOSFETs. Multiplying the gate charge by the on-resistance gives a figure of merit, providing a good balance between switching and resistive power dissipation.
- Slow transition times and oscillations on the voltage and current waveforms dissipate more power during the turn-on and turn-off of the low side MOSFET. A clean layout will minimize parasitic inductance and capacitance in the gate drive and high current paths. This will allow the fastest transition times and waveforms without oscillations. Low gate charge MOSFETs will switch faster than those with higher gate charge specifications.
- For the same size inductor, a lower value will have fewer turns and therefore, lower winding resistance. However, using too small of a value will increase the inductor current and therefore require more output capacitors to filter the output ripple.
- Lowering the current sense resistor value will decrease the power dissipated in the resistor. However, it will also increase the overcurrent limit and may require larger MOSFETs and inductor components to handle the higher currents.
- Use low ESR output capacitors to minimize the power dissipated in the capacitor's ESR.

Package Information



16-Pin SOIC (M)



16-Pin QSOP (QS)

MICREL INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com