MC10ELT25, MC100ELT25

-5V Differential ECL to TTL Translator

The MC10ELT/100ELT25 is a differential ECL to TTL translator. Because ECL levels are used, a +5 V, -5.2 V (or -4.5 V) and ground are required. The small outline 8-lead package and the single gate of the ELT25 makes it ideal for those applications where space, performance and low power are at a premium.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 2.6 ns Typical Propagation Delay
- 100 MHz F_{MAX} CLK
- 24 mA TTL Outputs
- Flow Through Pinouts
- Operating Range: V_{CC} = 4.5 V to 5.5 V with GND = 0 V; V_{EE} = -4.2 V to -5.7 V with GND = 0 V
- Internal Input Pulldown Resistors
- Q Output will default HIGH with inputs open or < 1.3 V

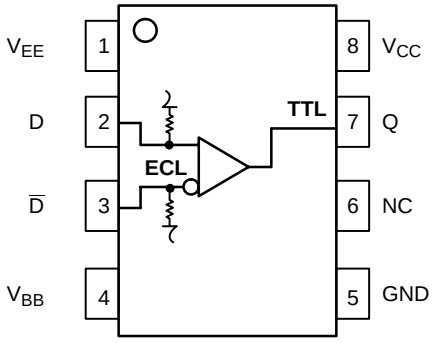

Figure 1. 8-Lead Pinout and Logic Diagram
(Top View)

PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	ECL Differential Inputs
Q	TTL Output
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground
NC	No Connect

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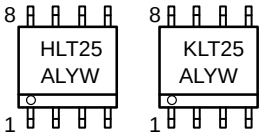
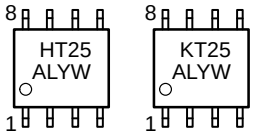
MARKING DIAGRAMS*

SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC10ELT25D	SO-8	98 Units/Rail
MC10ELT25DR2	SO-8	2500 Tape & Reel
MC100ELT25D	SO-8	98 Units/Rail
MC100ELT25DR2	SO-8	2500 Tape & Reel
MC10ELT25DT	TSSOP-8	98 Units/Rail
MC10ELT25DTR2	TSSOP-8	2500 Tape & Reel
MC100ELT25DT	TSSOP-8	98 Units/Rail
MC100ELT25DTR2	TSSOP-8	2500 Tape & Reel

†For additional tape and reel information, refer to Brochure BRD8011/D.

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistors		75 kΩ
Internal Input Pullup Resistors		N/A
ESD Protection	Human Body Model Machine Model	> 1 KV > 400 V
Moisture Sensitivity (Note 1)		Level 1
Flammability Rating Oxygen Index		UL-94 code V-0 @ 1/8” 28 to 34
Transistor Count		38 Devices
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. Refer to Application Note AND8003/D for additional information.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V	V_{EE} = -5.0 V	7	V
V_{EE}	Negative Power Supply	GND = 0 V	V_{CC} = +5.0 V	-8	V
V_{IN}	Input Voltage	GND = 0 V		0 to V_{EE}	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-8 SO-8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SO-8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES NECL INPUT DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = -5.0 V; GND = 0 V (Note 3)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 4)	-1230		-890	-1130		-810	-1060		-720	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Note 4)	-1950		-1500	-1950		-1480	-1950		-1445	mV
V_{BB}	Output Voltage Reference	-1.43		-1.30	-1.35		-1.25	-1.31		-1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Notes 4 and 5)	-2.8		0.0	-2.8		0.0	-2.8		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input parameters vary 1:1 with GND. V_{EE} can vary +0.06 V / -0.5 V.
4. TTL output R_L = 500 Ω to GND
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with GND.

100ELT SERIES NECL INPUT DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = -5.0 V; GND = 0 V (Note 6)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 7)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Note 7)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Notes 7 and 8)	-2.8		0.0	-2.8		0.0	-2.8		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

6. Input parameters vary 1:1 with GND. V_{EE} can vary +0.8 V / -0.5 V.
7. TTL output R_L = 500 Ω to GND
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with GND.

TTL OUTPUT DC CHARACTERISTICS V_{CC} = 4.5 V to 5.5 V; T_A = -40°C to +85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 9)	I_{OH} = -3.0 mA	2.4			V
V_{OL}	Output LOW Voltage (Note 9)	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current			11	16	mA
I_{CCL}	Power Supply Current			13	18	mA
I_{EE}	Negative Power Supply Current			15	21	mA
I_{OS}	Output Short Circuit Current		-150		-60	mA

9. TTL output R_L = 500 Ω to GND

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= -5.0 V; GND= 0 V (Note 10 and Note 11)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency					100					MHz
t_{PLH}	Propagation Delay @ 1.5 V	1.7		3.6	1.7		3.6	1.7		3.6	ns
t_{PHL}	Propagation Delay @ 1.5 V	2.6		4.1	2.6		4.1	2.6		4.1	ns
t_{JITTER}	Random Clock Jitter (RMS)					35					ps
t_r t_f	Output Rise/Fall Times QTTL 10% - 90%					1.9 2.3					ns
V_{PP}	Input Swing (Note 12)	200		1000	200		1000	200		1000	mV

10. V_{CC} can vary ± 0.25 V.
    V_{EE} can vary +0.06 V / -0.5 V for 10ELT; V_{EE} can vary +0.8 V / -0.5 V for 100ELT.
11. R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to Figure 2.
12. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40.

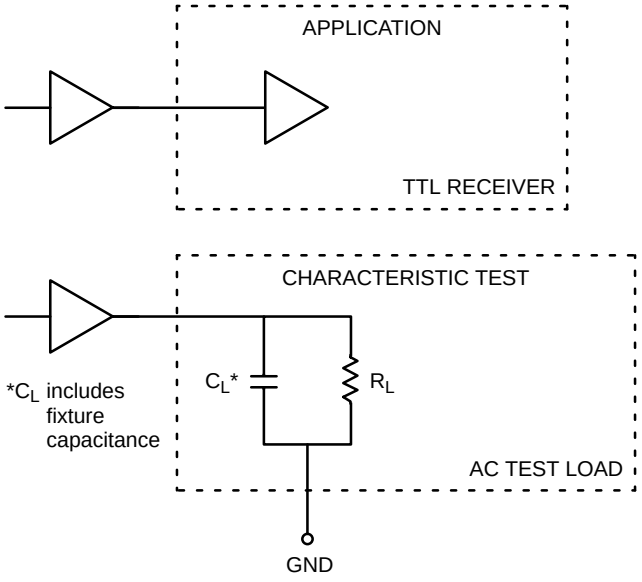


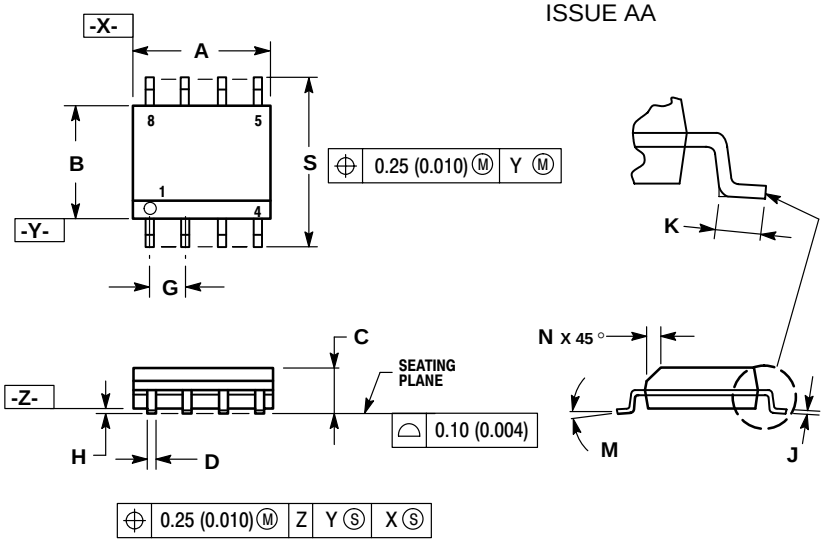
Figure 2. TTL Output Loading Used for Device Evaluation

Resource Reference of Application Notes

AN1404	-	ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
AN1405	-	ECL Clock Distribution Techniques
AN1406	-	Designing with PECL (ECL at +5.0 V)
AN1503	-	ECLinPS I/O SPICE Modeling Kit
AN1504	-	Metastability and the ECLinPS Family
AN1560	-	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	-	Interfacing Between LVDS and ECL
AN1596	-	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	-	Using Wire-OR Ties in ECLinPS Designs
AN1672	-	The ECL Translator Guide
AND8001	-	Odd Number Counters Design
AND8002	-	Marking and Date Codes
AND8020	-	Termination of ECL Logic Devices
AND8090	-	AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-07
ISSUE AA

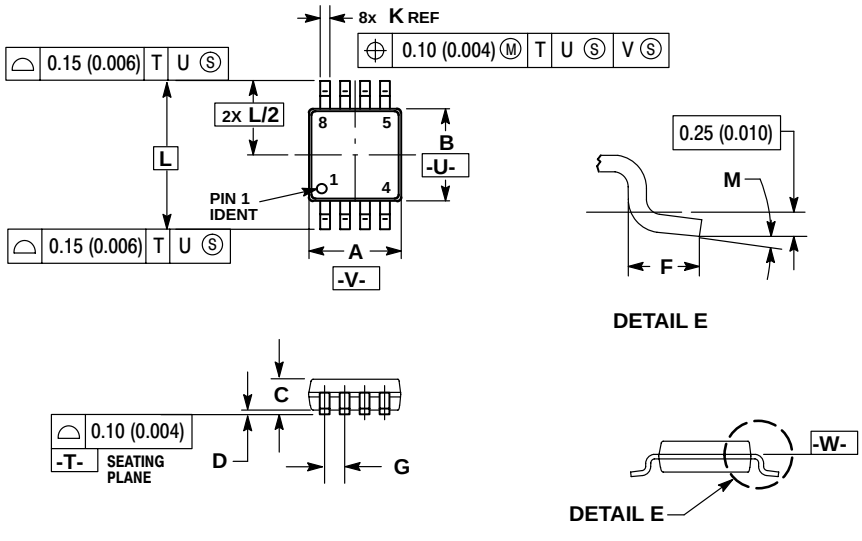


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDAARD IS 751−07

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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