

FEATURES

Low noise: 2.7 nV/ $\sqrt{\text{Hz}}$ @ $f = 10 \text{ kHz}$
Low offset voltage: 250 μV max over V_{CM}
Offset voltage drift: 0.4 $\mu\text{V}/^\circ\text{C}$ typ and 2.3 $\mu\text{V}/^\circ\text{C}$ max
Bandwidth: 28 MHz
Rail-to-rail input/output
Unity gain stable
2.7 V to 5.5 V operation
 -40°C to $+125^\circ\text{C}$ operation

APPLICATIONS

ADC and DAC buffers
Audio
Industrial controls
Precision filters
Digital scales
Strain gauges
PLL filters

GENERAL DESCRIPTION

The AD8655 is the industry's lowest noise, precision CMOS amplifier. It leverages the Analog Devices DigiTrim® technology to achieve high dc accuracy.

The AD8655 provides low noise (2.7 nV/ $\sqrt{\text{Hz}}$ @ 10 kHz), low THD + N (0.0007%), and high precision performance (250 μV max over V_{CM}) to low voltage applications. The ability to swing rail-to-rail at the input and output enables designers to buffer ADCs and other wide dynamic range devices in single-supply systems.

PIN CONFIGURATIONS

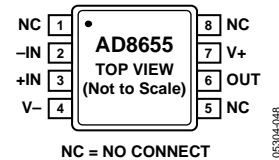


Figure 1. 8-Lead MSOP (RM-8)

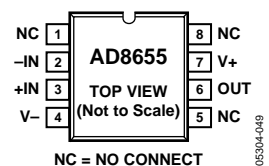


Figure 2. 8-Lead SOIC (R-8)

The AD8655 high precision performance improves the resolution and dynamic range in low voltage applications. Audio applications, such as microphone pre-amps and audio mixing consoles, benefit from the low noise, low distortion, and high output current capability of the AD8655 to reduce system level noise performance and maintain audio fidelity. The AD8655's high precision and rail-to-rail input and output benefit data acquisition, process controls, and PLL filter applications.

The AD8655 is fully specified over the -40°C to $+125^\circ\text{C}$ temperature range. The AD8655 is available in 8-lead MSOP and SOIC packages.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

AD8655

TABLE OF CONTENTS

5.0 V Electrical Specifications.....	3	Input Capacitance	15
2.7 V Electrical Specifications.....	4	Driving Capacitive Loads.....	15
Absolute Maximum Ratings.....	5	Layout, Grounding, and Bypassing Considerations	17
ESD Caution.....	5	Power Supply Bypassing	17
Typical Performance Characteristics	6	Grounding	17
Theory of Operation	14	Leakage Currents.....	17
Applications.....	15	Outline Dimensions	18
Input Overvoltage Protection	15	Ordering Guide	18

REVISION HISTORY

4/05—Revision 0: Initial Version

5.0 V ELECTRICAL SPECIFICATIONS

$V_S = 5.0\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V to }5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	250	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.4	2.3	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			300	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }5\text{ V}$	85	100		dB
Large Signal Voltage Gain	A_{VO}	$V_O = 0.2\text{ V to }4.8\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{CM} = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	110		dB
			95			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$; $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.97	4.991		V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$; $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		8	30	mV
Output Current	I_{OUT}	$V_{OUT} = \pm 0.5\text{ V}$		± 220		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }5.0\text{ V}$	88	105		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		3.7	4.5	mA
					5.3	mA
INPUT CAPACITANCE						
Differential	C_{IN}			9.3		pF
Common-Mode				16.7		pF
NOISE PERFORMANCE						
Input Voltage Noise Density	e_n	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		4		$\text{nV}/\sqrt{\text{Hz}}$
Total Harmonic Distortion + Noise	THD + N	$G = 1$, $R_L = 1\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 2\text{ V p-p}$		2.7		$\text{nV}/\sqrt{\text{Hz}}$
				0.0007		%
FREQUENCY RESPONSE						
Gain Bandwidth Product	GBP			28		MHz
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		11		$\text{V}/\mu\text{s}$
Settling Time	t_s	To 0.1%, $V_{IN} = 0\text{ V to }2\text{ V step}$, $G = +1$		370		ns
Phase Margin		$C_L = 0\text{ pF}$		69		degrees

AD8655

2.7 V ELECTRICAL SPECIFICATIONS

$V_S = 2.7\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V to }2.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		44	250	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.4	2.0	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			300	pA
Input Voltage Range			0		10	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }2.7\text{ V}$	80	98	300	pA
Large Signal Voltage Gain	A_{VO}	$V_O = 0.2\text{ V to }2.5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{CM} = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	98		2.7	V
			90			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$; $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.67	2.688		V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$; $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	30	mV
Output Current	I_{OUT}	$V_{OUT} = \pm 0.5\text{ V}$		± 75		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }5.0\text{ V}$	88	105		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		3.7	4.5	mA
					5.3	mA
INPUT CAPACITANCE						
Differential	C_{IN}			9.3		pF
Common-Mode				16.7		pF
NOISE PERFORMANCE						
Input Voltage Noise Density	e_n	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		4.0		$\text{nV}/\sqrt{\text{Hz}}$
Total Harmonic Distortion + Noise	THD + N	$G = 1$, $R_L = 1\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 2\text{ V p-p}$		2.7		$\text{nV}/\sqrt{\text{Hz}}$
				0.0007		%
FREQUENCY RESPONSE						
Gain Bandwidth Product	GBP			27		MHz
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		8.5		$\text{V}/\mu\text{s}$
Settling Time	t_s	To 0.1%, $V_{IN} = 0\text{ to }1\text{ V step}$, $G = +1$		370		ns
Phase Margin		$C_L = 0\text{ pF}$		54		degrees

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	VSS – 0.3 V to VDD + 0.3 V
Differential Input Voltage	±6 V
Output Short-Circuit Duration to GND	Indefinite
Electrostatic Discharge (HBM)	3.0 kV
Storage Temperature Range R, RM Packages	–65°C to +150°C
Junction Temperature Range R, RM Packages	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4.

Package Type	θ_{JA} ¹	θ_{JC}	Unit
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC (R)	158	43	°C/W

¹ θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for a device soldered in the circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

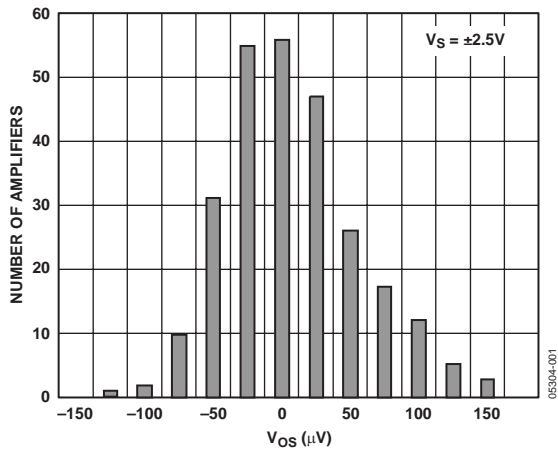


Figure 3. Input Offset Voltage Distribution

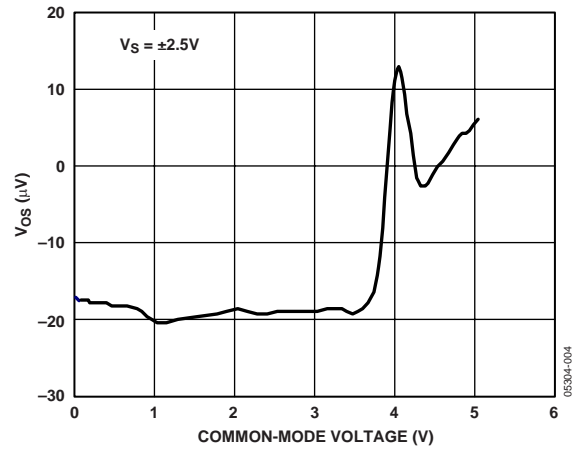


Figure 6. Input Offset Voltage vs. Common-Mode Voltage

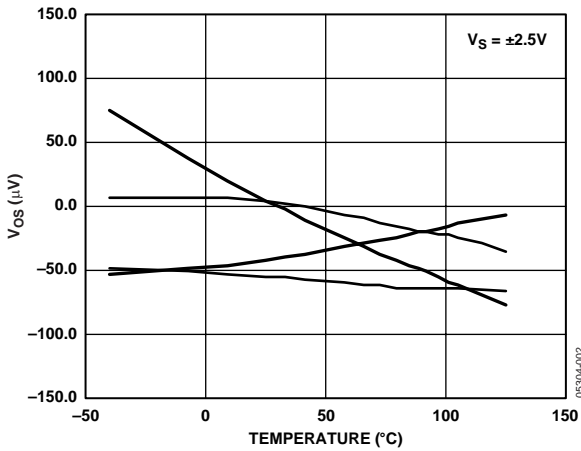


Figure 4. Input Offset Voltage vs. Temperature

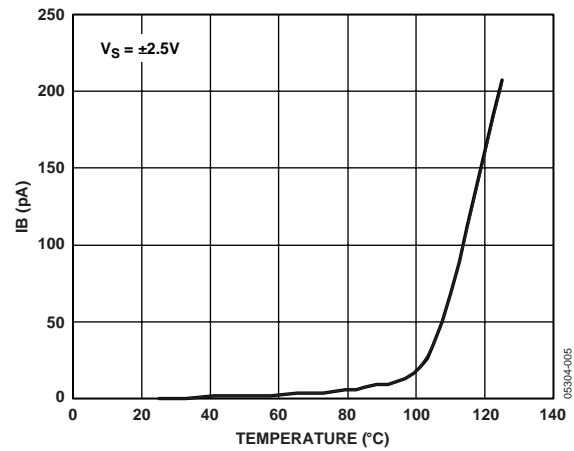


Figure 7. Input Bias Current vs. Temperature

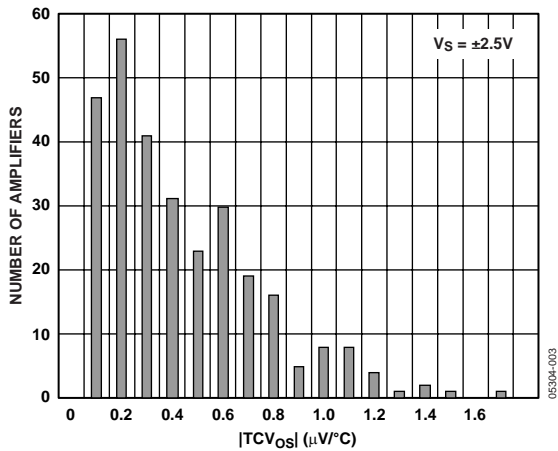


Figure 5. $|TCV_{OS}|$ Distribution

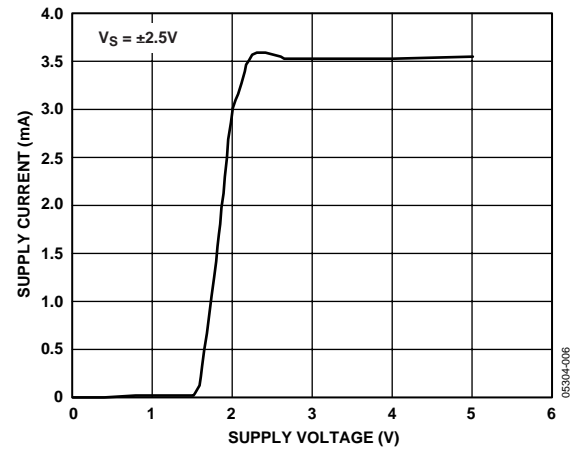


Figure 8. Supply Current vs. Supply Voltage

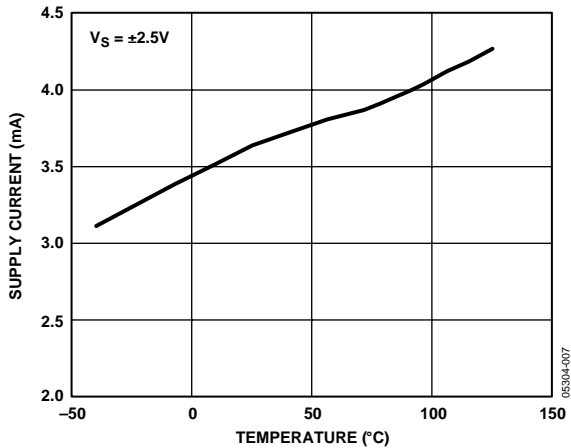


Figure 9. Supply Current vs. Temperature

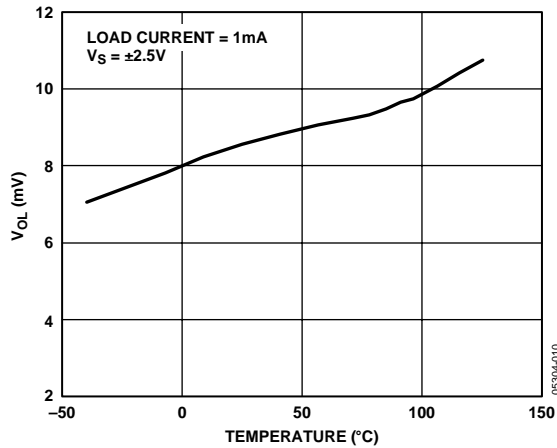


Figure 12. Output Voltage Swing Low vs. Temperature

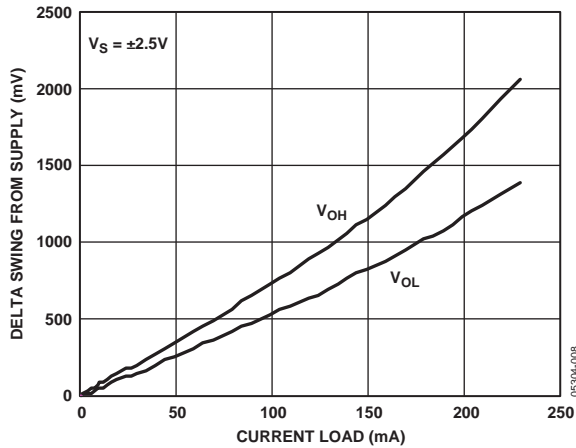


Figure 10. Output Voltage to Supply Rail vs. Current Load

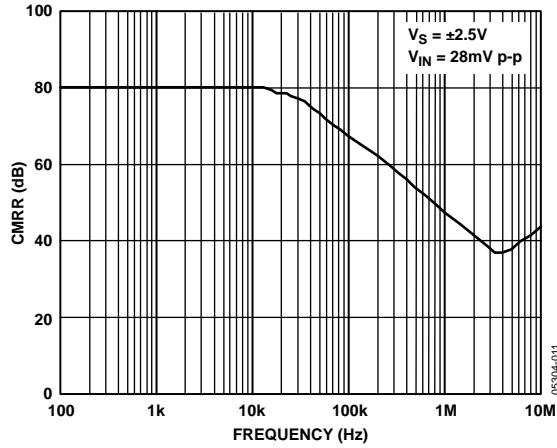


Figure 13. Small Signal CMRR vs. Frequency

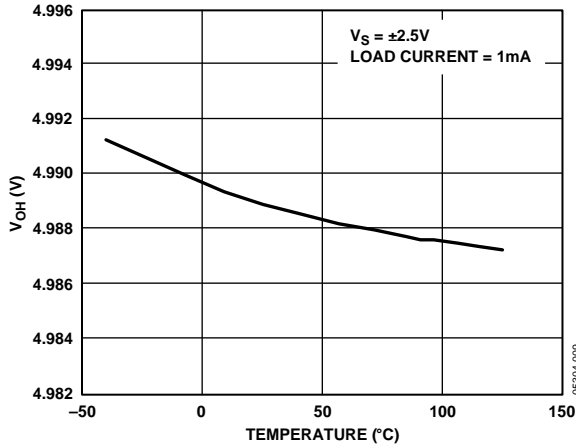


Figure 11. Output Voltage Swing High vs. Temperature

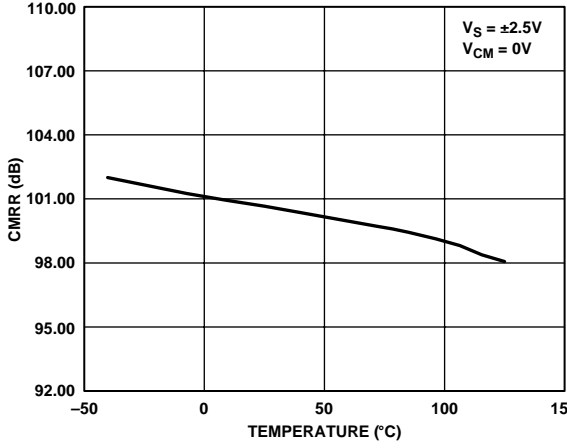


Figure 14. Large Signal CMRR vs. Temperature

AD8655

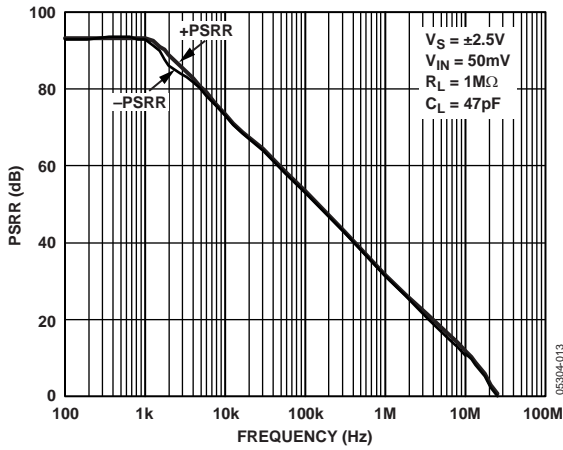


Figure 15. Small Signal PSRR vs. Frequency

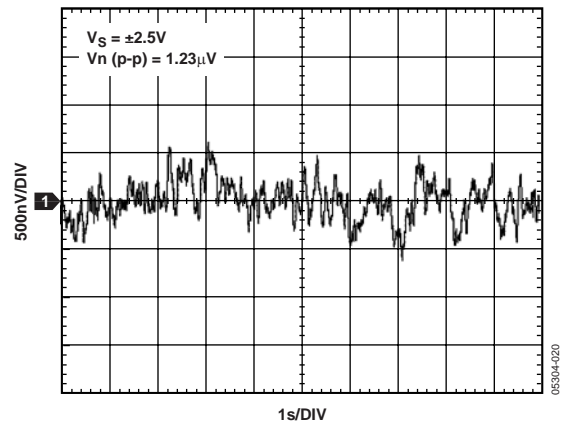


Figure 18. Low Frequency Noise (0.1 Hz to 10 Hz).

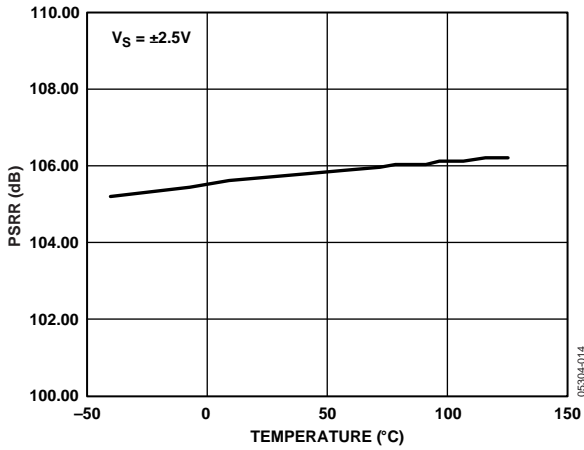


Figure 16. Large Signal PSRR vs. Temperature

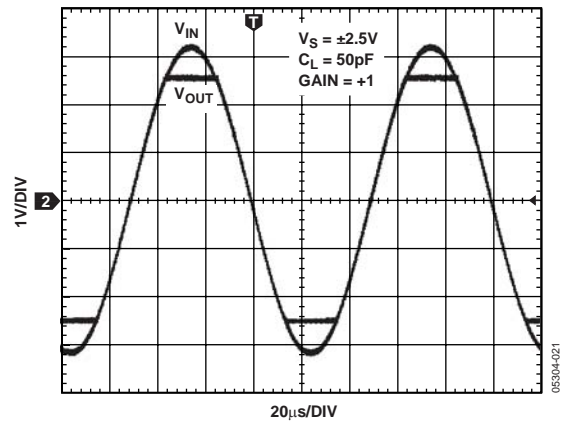


Figure 19. No Phase Reversal

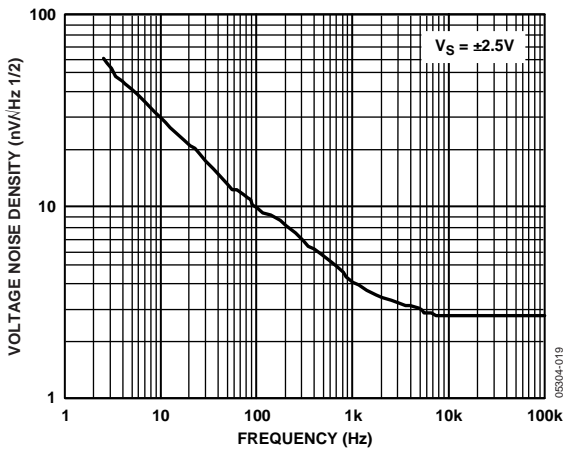


Figure 17. Voltage Noise Density vs. Frequency

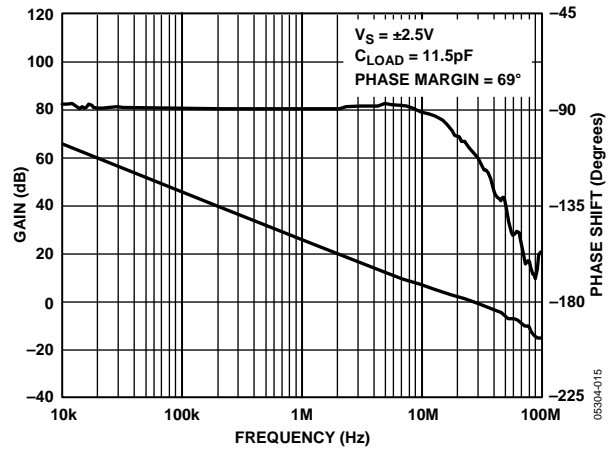


Figure 20. Open-Loop Gain and Phase vs. Frequency

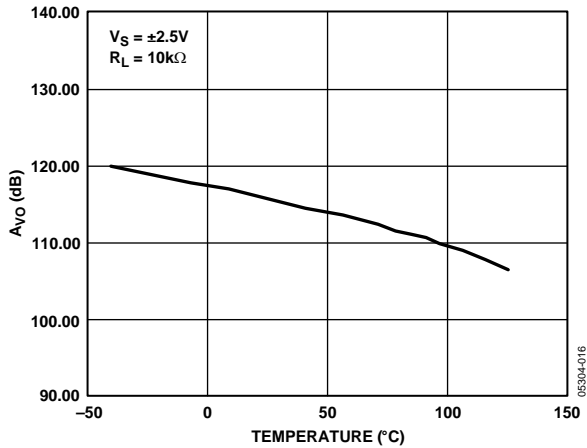


Figure 21. Large Signal Open-Loop Gain vs. Temperature

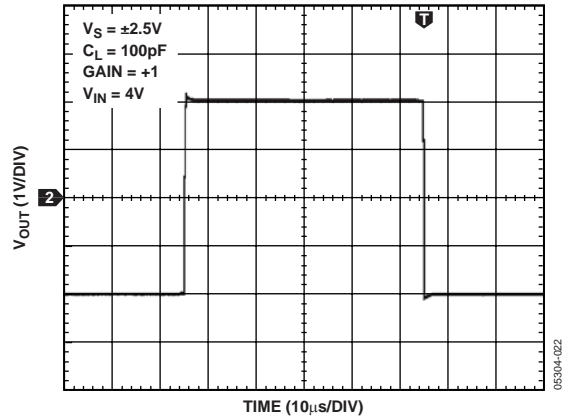


Figure 24. Large Signal Response

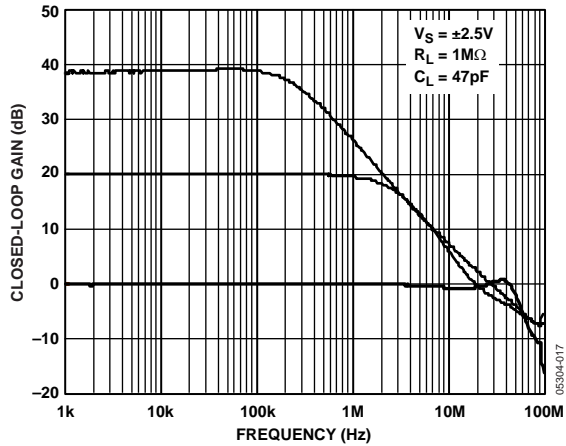


Figure 22. Closed-Loop Gain vs. Frequency

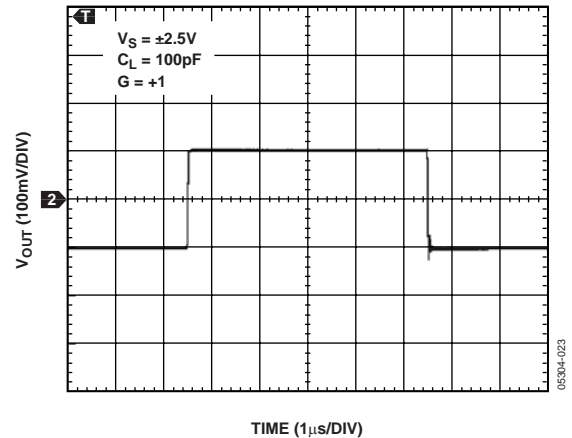


Figure 25. Small Signal Response

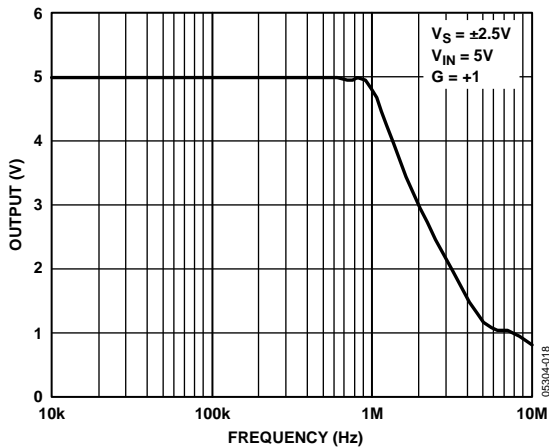


Figure 23. Maximum Output Swing vs. Frequency

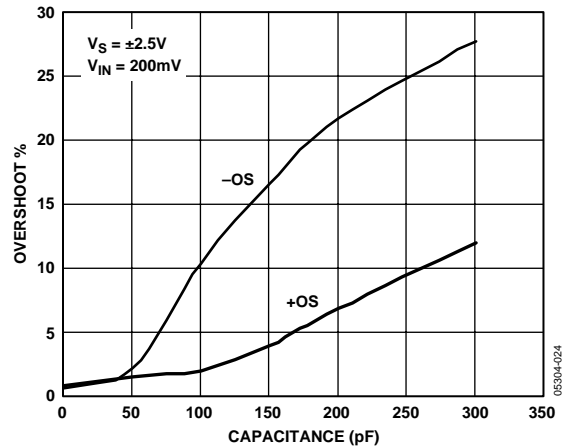


Figure 26. Small Signal Overshoot vs. Load Capacitance

AD8655

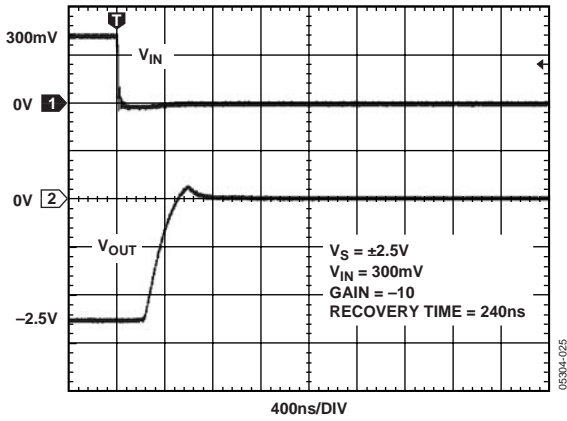


Figure 27. Negative Overload Recovery Time

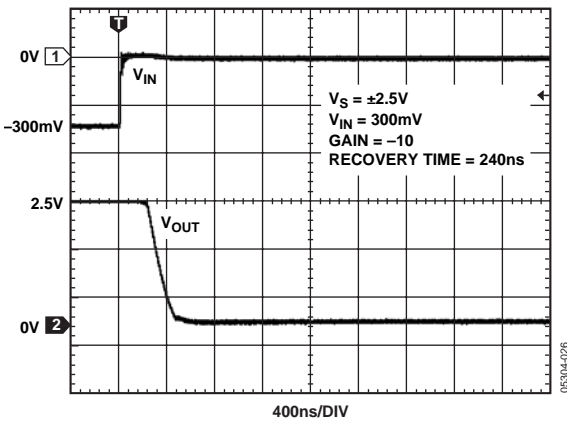


Figure 28. Positive Overload Recovery Time

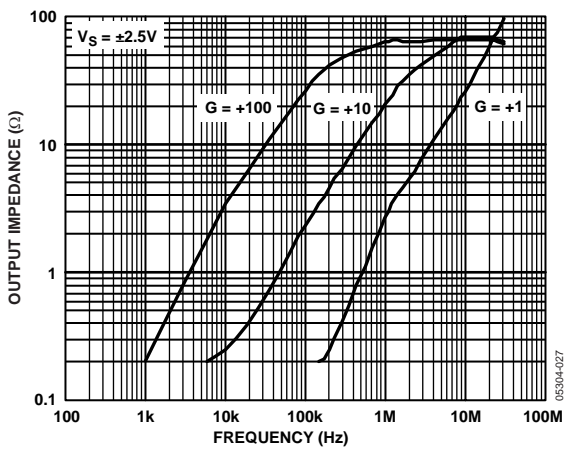


Figure 29. Output Impedance vs. Frequency

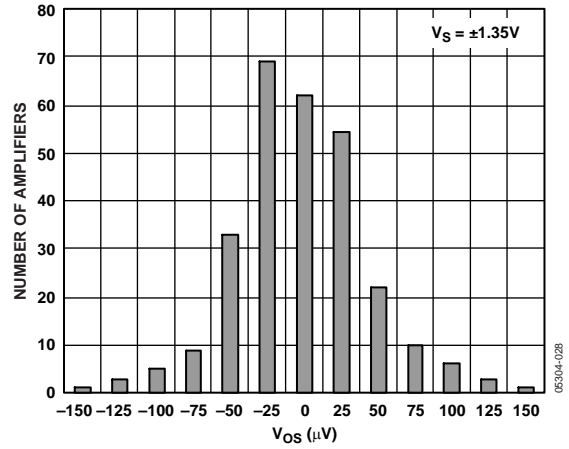


Figure 30. Input Offset Voltage Distribution

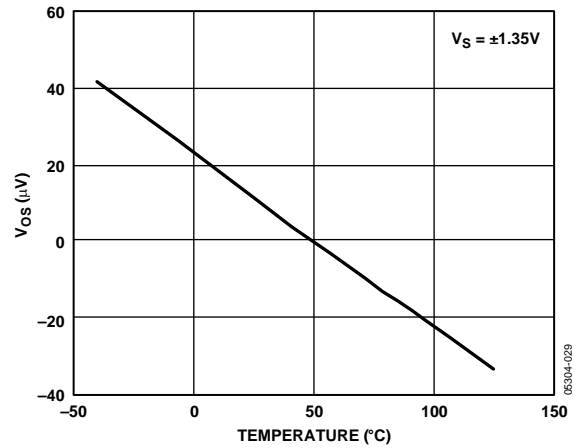


Figure 31. Input Offset Voltage vs. Temperature

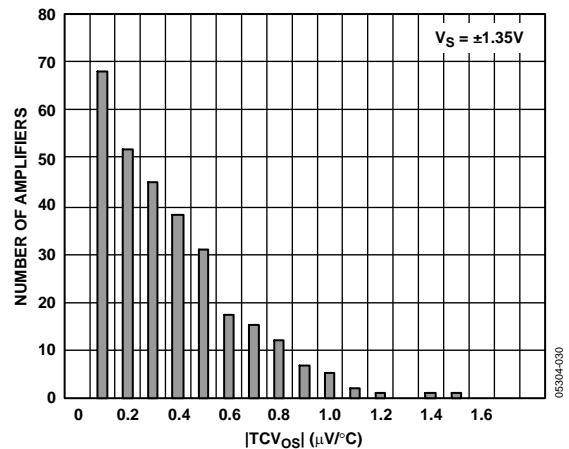


Figure 32. $|TCV_{OS}|$ Distribution

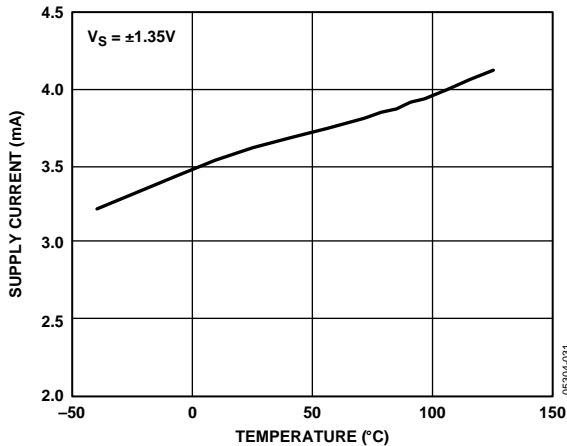


Figure 33. Supply Current vs. Temperature

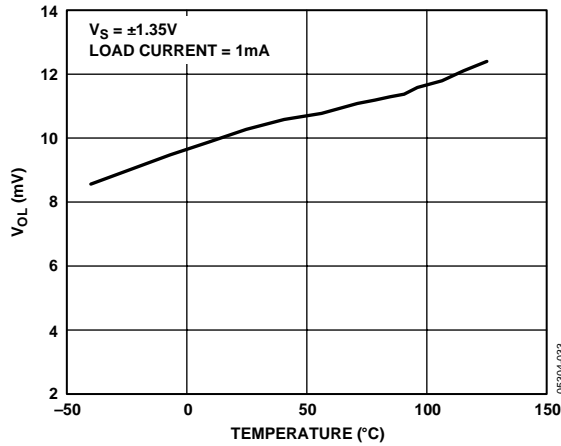


Figure 36. Output Voltage Swing Low vs. Temperature

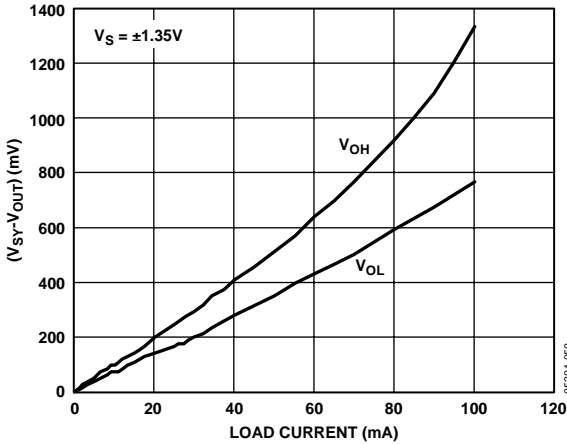


Figure 34. Output Voltage to Supply Rail vs. Load Current

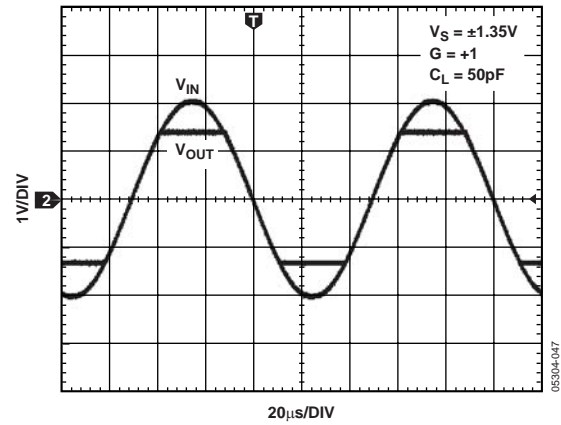


Figure 37. No Phase Reversal

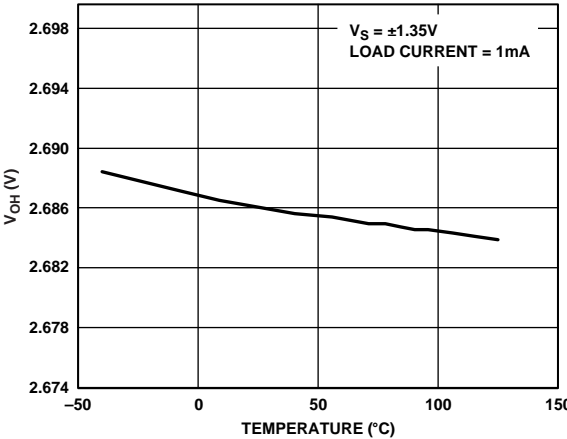


Figure 35. Output Voltage Swing High vs. Temperature

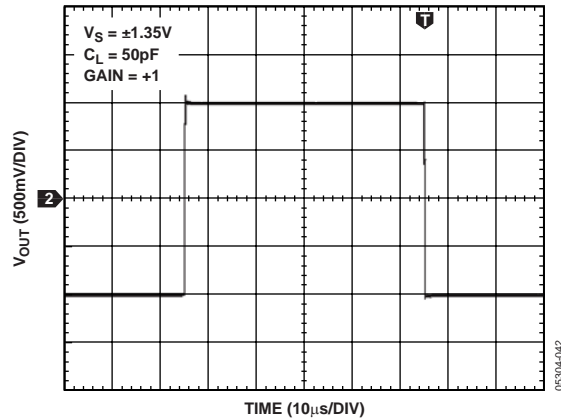


Figure 38. Large Signal Response

AD8655

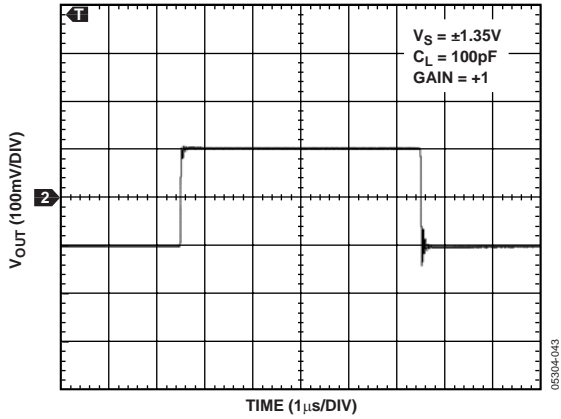


Figure 39. Small Signal Response

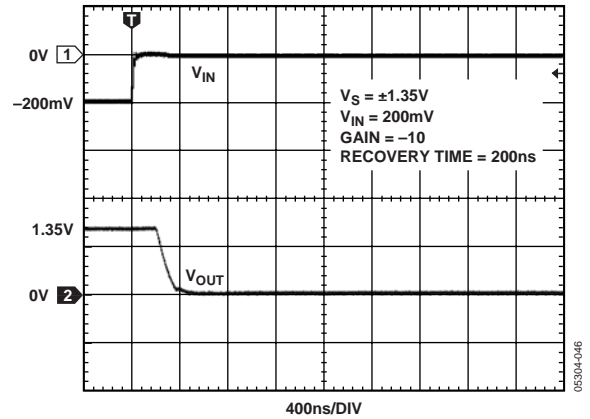


Figure 42. Positive Overload Recovery Time

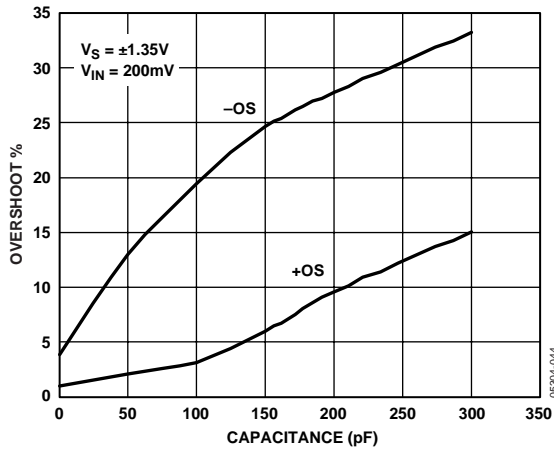


Figure 40. Small Signal Overshoot vs. Load Capacitance

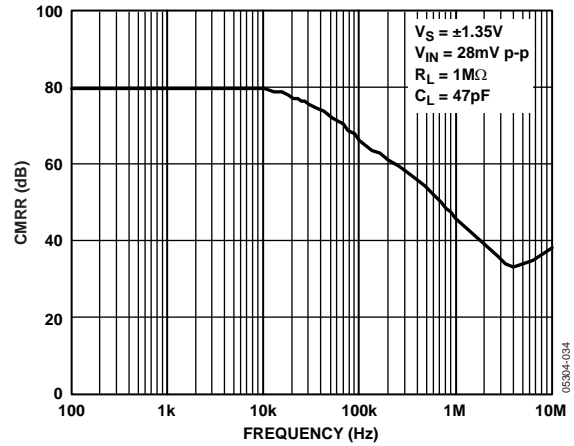


Figure 43. Small Signal CMRR vs. Frequency

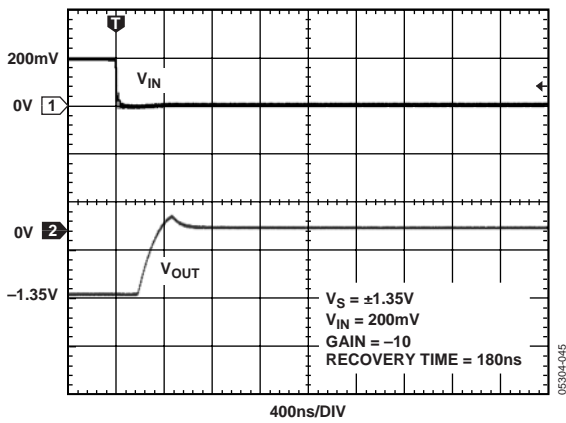


Figure 41. Negative Overload Recovery Time

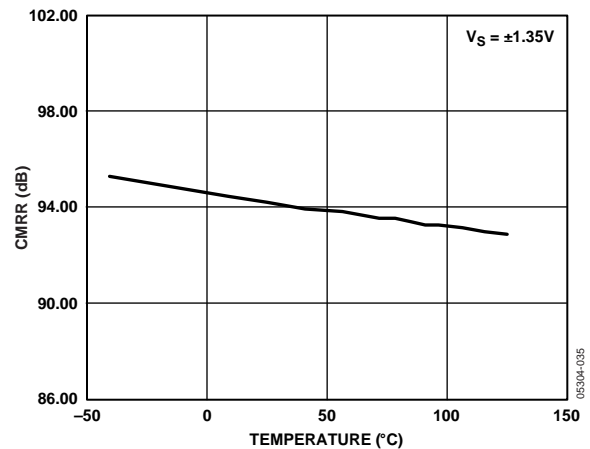


Figure 44. Large Signal CMRR vs. Temperature

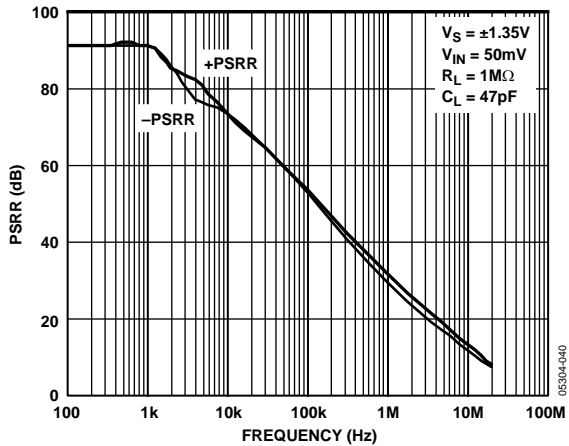


Figure 45. Small Signal PSSR vs. Frequency

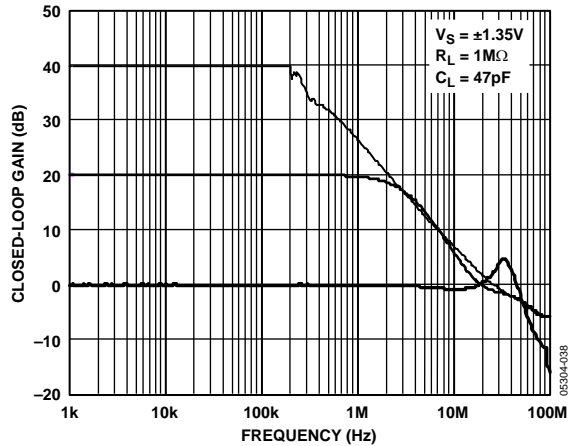


Figure 48. Closed-Loop Gain vs. Frequency

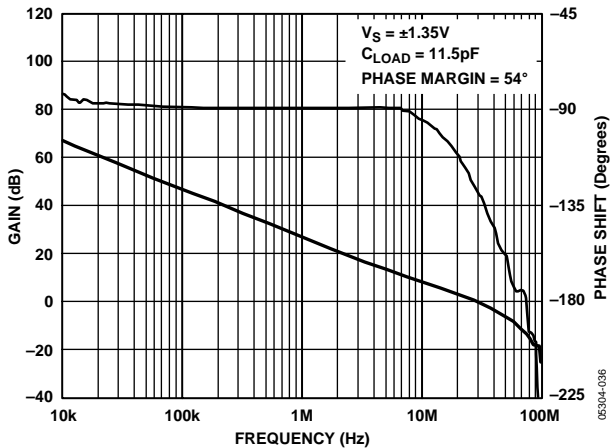


Figure 46. Open-Loop Gain and Phase vs. Frequency

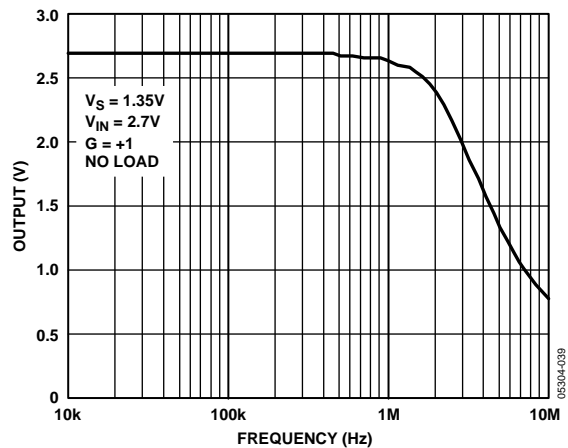


Figure 49. Maximum Output Swing vs. Frequency

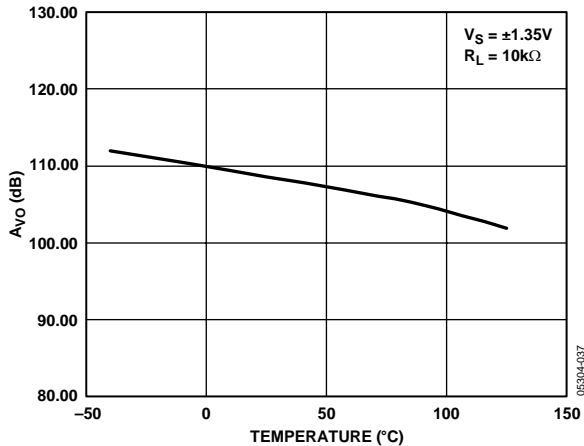


Figure 47. Large Signal Open-Loop Gain vs. Temperature

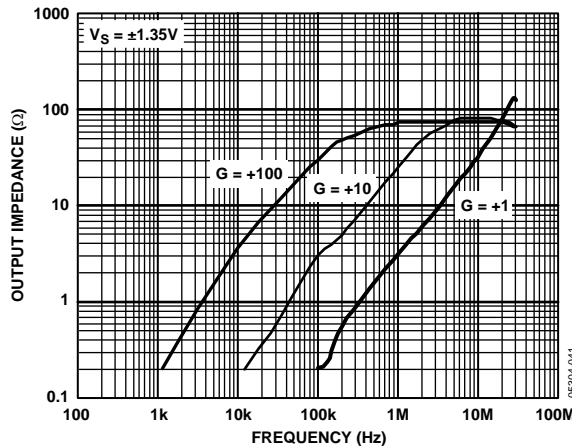


Figure 50. Output Impedance vs. Frequency

THEORY OF OPERATION

The AD8655 amplifier is a voltage feedback, rail-to-rail input and output precision CMOS amplifier, which operates from 2.7 V to 5.0 V of power supply voltage. This amplifier uses the Analog Devices DigiTrim technology to achieve a higher degree of precision than is available from most CMOS amplifiers. DigiTrim technology, used in a number of ADI amplifiers, is a method of trimming the offset voltage of the amplifier after it is packaged. The advantage of post-package trimming is that it corrects any offset voltages caused by the mechanical stresses of assembly.

The AD8655 is available in a standard op amp pinout, making DigiTrim completely transparent to the user. The input stage of the amplifier is a true rail-to-rail architecture, allowing the input common-mode voltage range of the amplifier to extend to both positive and negative supply rails. The open-loop gain of the AD8655 with a load of 10 k Ω is typically 110 dB.

The AD8655 can be used in any precision op amp application. The amplifier does not exhibit phase reversal for common-mode voltages within the power supply. The AD8655 is a great choice for high resolution data acquisition systems with voltage noise of 2.7 nV/ $\sqrt{\text{Hz}}$ and THD + Noise of -103 dB for a 2 V p-p signal at 10 kHz. Its low noise, sub-pA input bias current, precision offset, and high speed make it a superb preamp for fast filter applications. The speed and output drive capability of the AD8655 also make it useful in video applications.

APPLICATIONS

INPUT OVERVOLTAGE PROTECTION

The internal protective circuitry of the AD8655 allows voltages exceeding the supply to be applied at the input. It is recommended, however, not to apply voltages that exceed the supplies by more than 0.3 V at either input of the amplifier. If a higher input voltage is applied, series resistors should be used to limit the current flowing into the inputs. The input current should be limited to less than 5 mA.

The extremely low input bias current allows the use of larger resistors, which allows the user to apply higher voltages at the inputs. The use of these resistors adds thermal noise, which contributes to the overall output voltage noise of the amplifier. For example, a 10 kΩ resistor has less than 12.6 nV/√Hz of thermal noise and less than 10 nV of error voltage at room temperature.

INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. For circuits with resistive feedback network, the total capacitance, whether it is the source capacitance, stray capacitance on the input pin, or the input capacitance of the amplifier causes a breakpoint in the noise gain of the circuit. As a result, a capacitor must be added in parallel with the gain resistor to obtain stability. The noise gain is a function of frequency and peaks at the higher frequencies, assuming the feedback capacitor is selected to make the second-order system critically damped. A few picofarads of capacitance at the input reduce the input impedance at high frequencies, which increases the amplifier's gain, causing peaking in the frequency response or oscillations. With the AD8655, additional input damping is required for stability with capacitive loads greater than 200 pF with direct input to output feedback. See the next section on Driving Capacitive Loads.

DRIVING CAPACITIVE LOADS

Although the AD8655 can drive capacitive loads up to 500 pF without oscillating, a large amount of ringing is present when operating the part with input frequencies above 100 kHz. This is especially true when the amplifier is configured in positive unity gain (worst case). When such large capacitive loads are required, the use of external compensation is highly recommended. This reduces the overshoot and minimizes ringing, which in turn, improves the stability of the AD8655 when driving large capacitive loads.

One simple technique for compensation is a snubber that consists of a simple RC network. With this circuit in place, output swing is maintained, and the amplifier is stable at all gains. Figure 52 shows the implementation of a snubber, which reduces overshoot by more than 30% and eliminates ringing. Using a snubber does not recover the loss of bandwidth incurred from a heavy capacitive load.

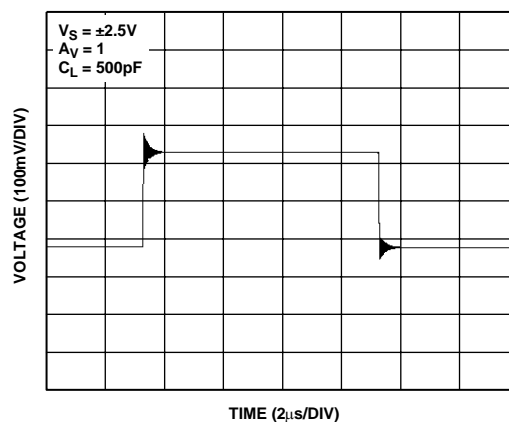


Figure 51. Driving Heavy Capacitive Loads Without Compensation

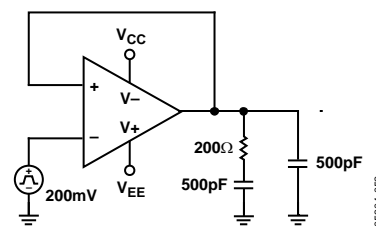


Figure 52. Snubber Network

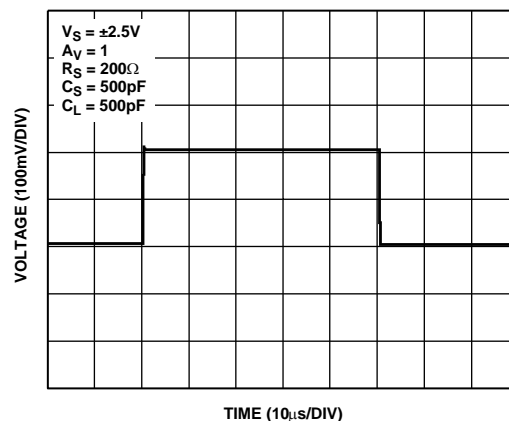


Figure 53. Driving Heavy Capacitive Loads Using a Snubber Network

AD8655

THD Readings vs. Common-Mode Voltage

Total harmonic distortion of the AD8655 is well below 0.0007% with a load of 1 k Ω . The distortion is a function of the circuit configuration, the voltage applied, and the layout, in addition to other factors.

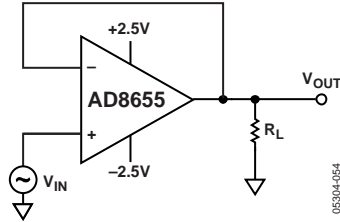


Figure 54. THD + N Test Circuit

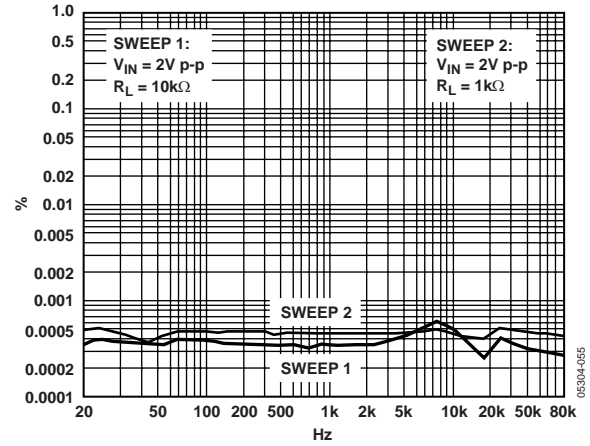


Figure 55. THD + Noise vs. Frequency

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

POWER SUPPLY BYPASSING

Power supply pins can act as inputs for noise, so care must be taken to apply a noise-free, stable dc voltage. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering most of the noise. Bypassing schemes are designed to minimize the supply impedance at all frequencies with a parallel combination of capacitors with values of 0.1 μF and 4.7 μF . Chip capacitors of 0.1 μF (X7R or NPO) are critical and should be as close as possible to the amplifier package. The 4.7 μF tantalum capacitor is less critical for high frequency bypassing, and, in most cases, only one is needed per board at the supply inputs.

GROUNDING

A ground plane layer is important for densely packed PC boards to minimize parasitic inductances. This minimizes voltage drops with changes in current. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances, and, therefore, the high frequency impedance of the path. Large changes in currents in an inductive ground return create unwanted voltage noise.

The length of the high frequency bypass capacitor leads is critical, and, therefore, surface-mount capacitors are recommended. A parasitic inductance in the bypass ground trace works against the low impedance created by the bypass capacitor. Because load currents flow from the supplies, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For larger value capacitors intended to be effective at lower frequencies, the current return path distance is less critical.

LEAKAGE CURRENTS

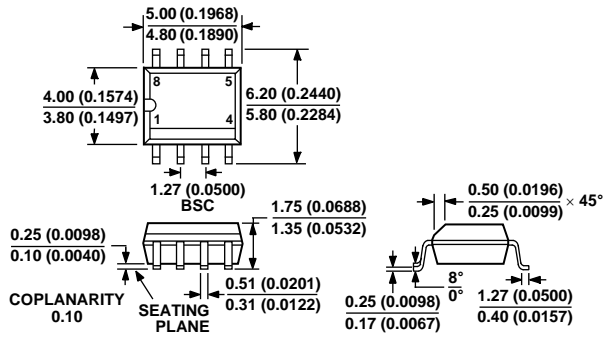
Poor PC board layout, contaminants, and the board insulator material can create leakage currents that are much larger than the input bias current of the AD8655. Any voltage differential between the inputs and nearby traces sets up leakage currents through the PC board insulator, for example, $1\text{ V}/100\text{ G}\Omega = 10\text{ pA}$. Similarly, any contaminants on the board can create significant leakage (skin oils are a common problem).

To significantly reduce leakage, put a guard ring (shield) around the inputs and input leads that are driven to the same voltage potential as the inputs. This ensures that there is no voltage potential between the inputs and the surrounding area to set up any leakage currents. To be effective, the guard ring must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above and below, by using a multilayer board.

The charge absorption of the insulator material itself can also cause leakage currents. Minimizing the amount of material between the input leads and the guard ring helps to reduce the absorption. Also, low absorption materials, such as Teflon® or ceramic, may be necessary in some instances.

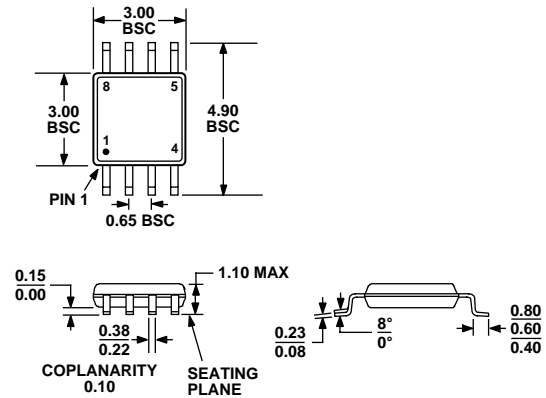
AD8655

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 56. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187AA

Figure 57. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8655ARZ ¹	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC)	R-8	
AD8655ARZ-REEL ¹	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC)	R-8	
AD8655ARZ-REEL7 ¹	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC)	R-8	
AD8655ARMZ-REEL ¹	-40°C to +125°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	A0D
AD8655ARMZ-R2 ¹	-40°C to +125°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	A0D

¹ Z = Pb-free part.

NOTES

AD8655

NOTES