

# FCD5N60 / FCU5N60

## 600V N-Channel MOSFET

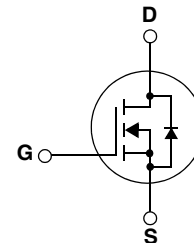
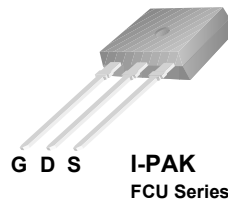
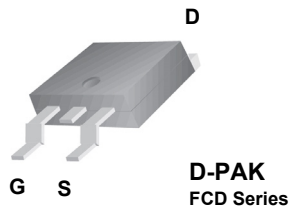
### Features

- 650V @ $T_J = 150^\circ\text{C}$
- Typ.  $R_{ds(on)} = 0.81\Omega$
- Ultra low gate charge (typ.  $Q_g = 16\text{nC}$ )
- Low effective output capacitance (typ.  $C_{oss,eff} = 32\text{pF}$ )
- 100% avalanche tested

### Description

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



### Absolute Maximum Ratings

Symbol	Parameter	FCD5N60 / FCU5N60	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	4.6 2.9	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	13.8	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	2.9	mJ
$I_{AR}$	Avalanche Current (Note 1)	4.6	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.4	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	20	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	54 0.43	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FCD5N60/FCU5N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	83	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD5N60	FCD5N60TM	D-PAK	380mm	16mm	2500
FCD5N60	FCD5N60TF	D-PAK	380mm	16mm	2000
FCU5N60	FCU5N60	I-PAK	--	--	70

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

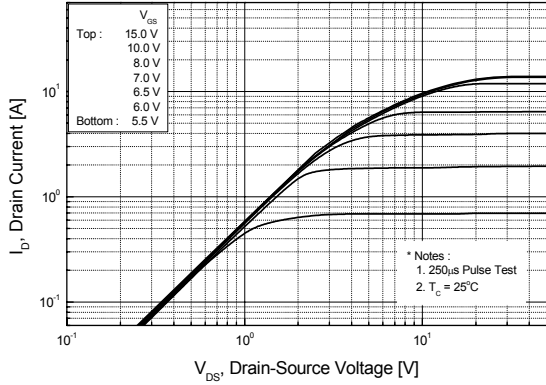
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250 $\mu$ A, T <sub>J</sub> = 25 $^\circ$ C	600	--	--	V
		V <sub>GS</sub> = 0V, I <sub>D</sub> = 250 $\mu$ A, T <sub>J</sub> = 150 $^\circ$ C	--	650	--	V
$\Delta$ BV <sub>DSS</sub> / $\Delta$ T <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 $\mu$ A, Referenced to 25 $^\circ$ C	--	0.6	--	V/ $^\circ$ C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 4.6A	--	700	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V	--	--	1	$\mu$ A
		V <sub>DS</sub> = 480V, T <sub>C</sub> = 125 $^\circ$ C	--	--	10	$\mu$ A
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 $\mu$ A	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.3A	--	0.81	0.95	$\Omega$
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 2.3A (Note 4)	--	3.8	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	470	600	pF
C <sub>oss</sub>	Output Capacitance		--	250	320	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	22	--	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	12	--	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0V to 400V, V <sub>GS</sub> = 0V	--	32	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 4.6A R <sub>G</sub> = 25 $\Omega$	--	12	30	ns
t <sub>r</sub>	Turn-On Rise Time		--	40	90	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	47	95	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4, 5)	--	22	55
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 4.6A V <sub>GS</sub> = 10V	--	16	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	2.8	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4, 5)	--	7	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	4.6	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	13.8	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 4.6A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 4.6A dI <sub>F</sub> /dt = 100A/ $\mu$ s (Note 4)	--	295	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	2.7	--	$\mu$ C

### NOTES:

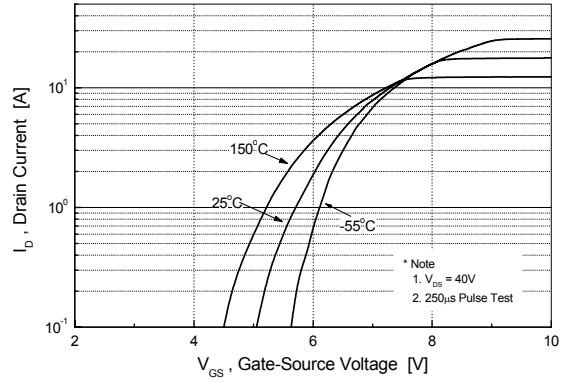
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 2.3A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 $\Omega$ , Starting T<sub>J</sub> = 25 $^\circ$ C
3. I<sub>SD</sub>  $\leq$  4.6A, di/dt  $\leq$  1200A/ $\mu$ s, V<sub>DD</sub>  $\leq$  BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25 $^\circ$ C
4. Pulse Test: Pulse width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

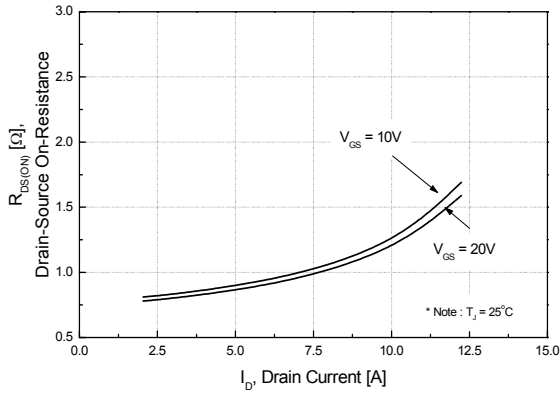
**Figure 1. On-Region Characteristics**



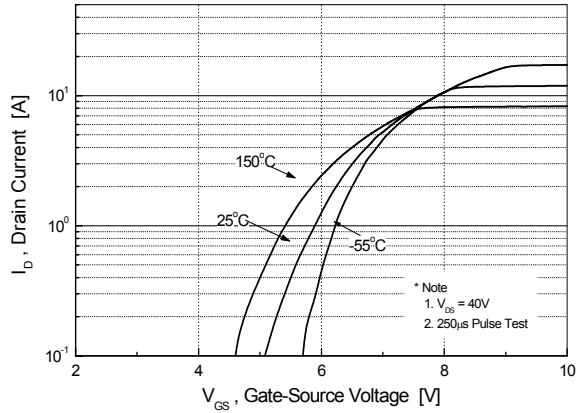
**Figure 2. Transfer Characteristics**



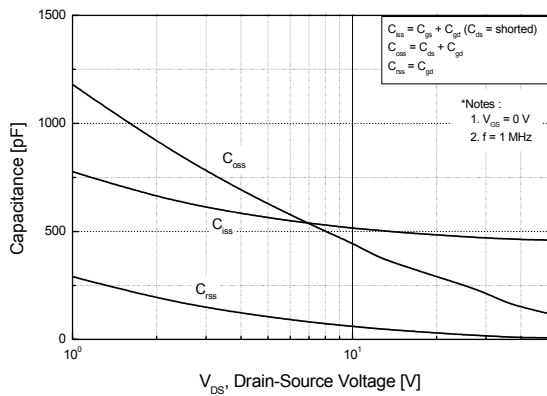
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



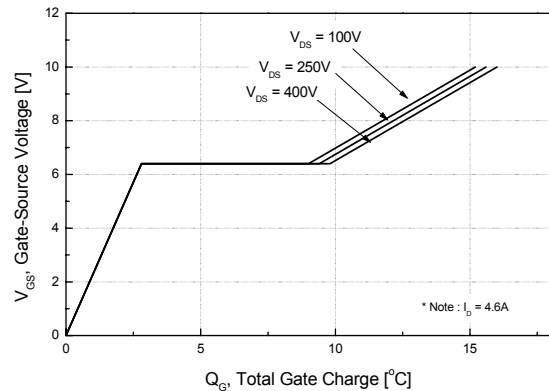
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

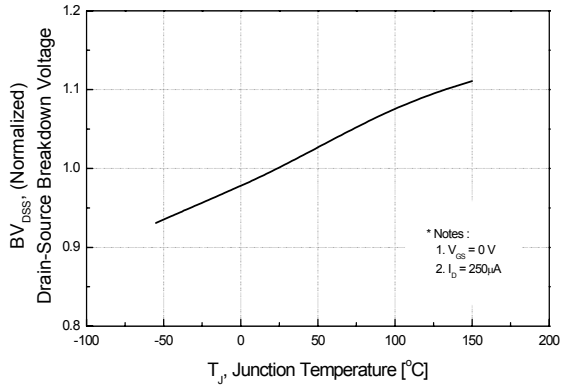


**Figure 6. Gate Charge Characteristics**

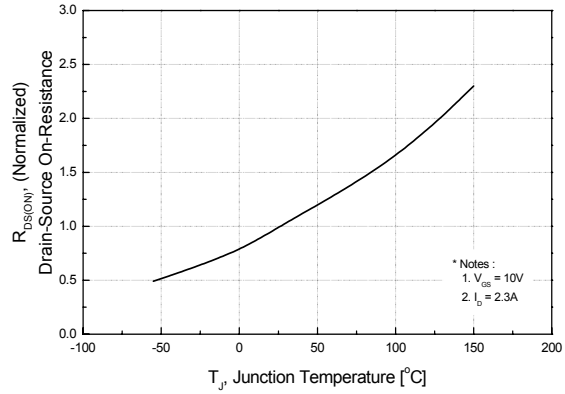


## Typical Performance Characteristics (Continued)

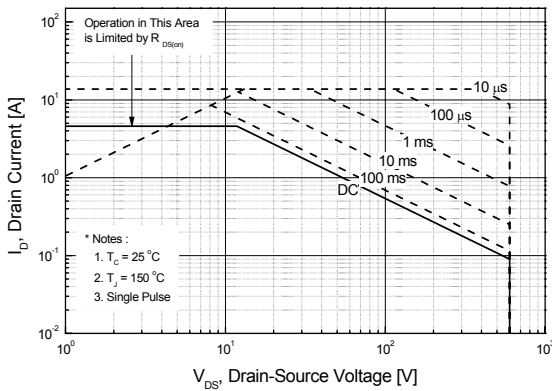
**Figure 7. Breakdown Voltage Variation vs. Temperature**



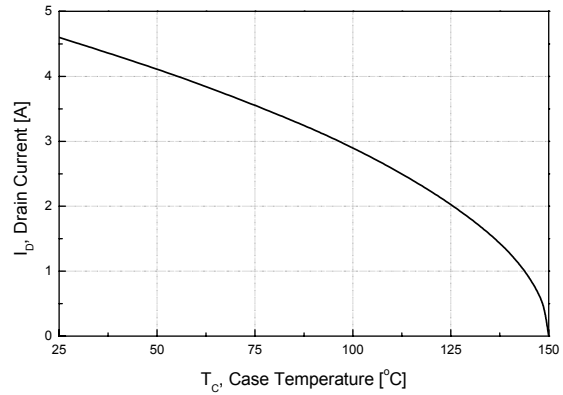
**Figure 8. On-Resistance Variation vs. Temperature**



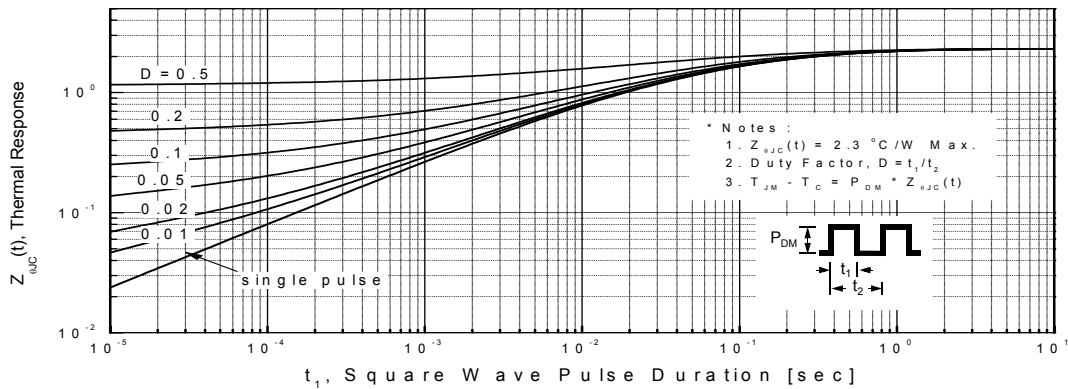
**Figure 9. Maximum Safe Operating Area**



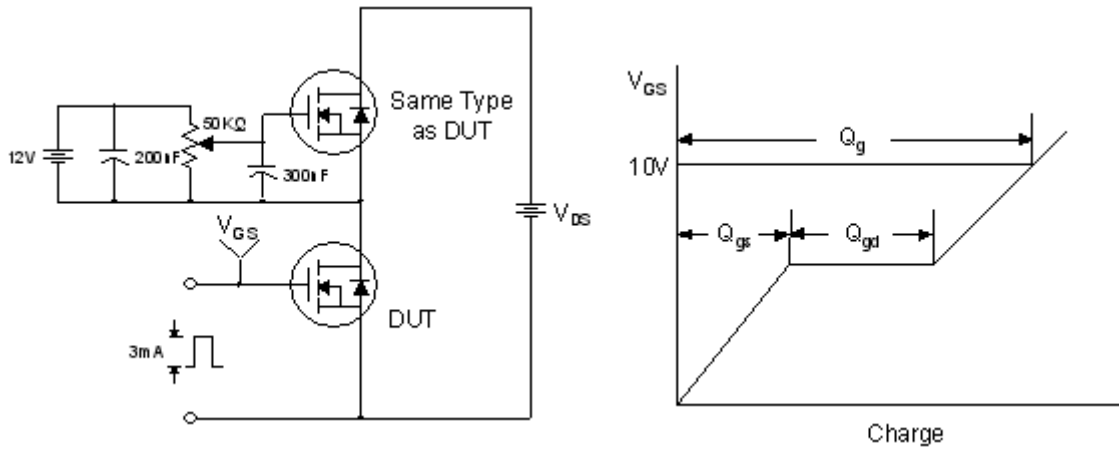
**Figure 10. Maximum Drain Current vs. Case Temperature**



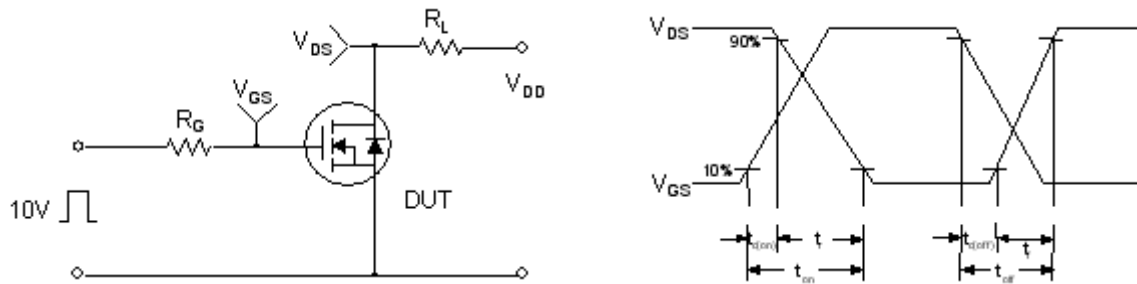
**Figure 11. Transient Thermal Response Curve**



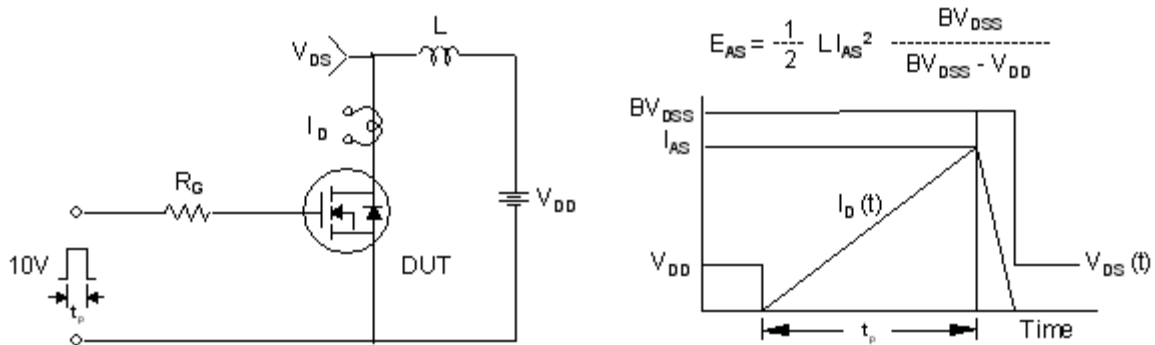
**Gate Charge Test Circuit & Waveform**



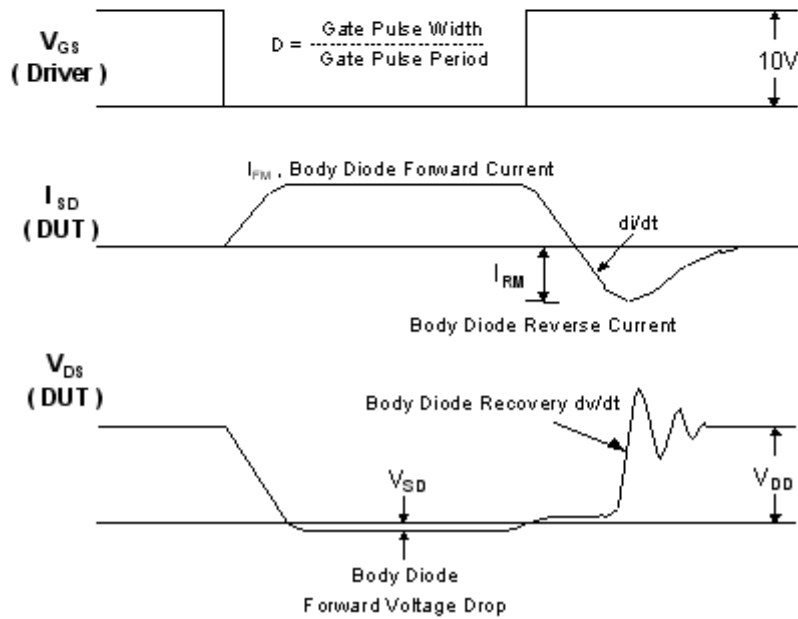
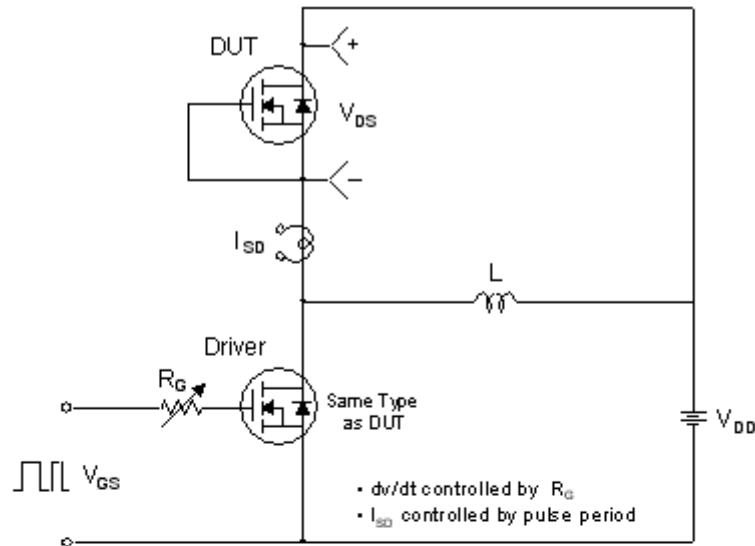
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

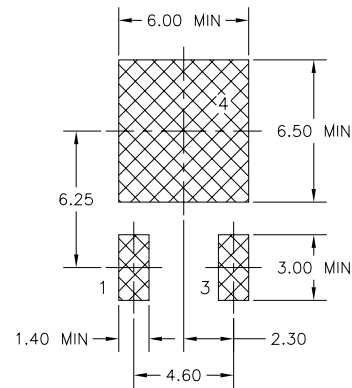
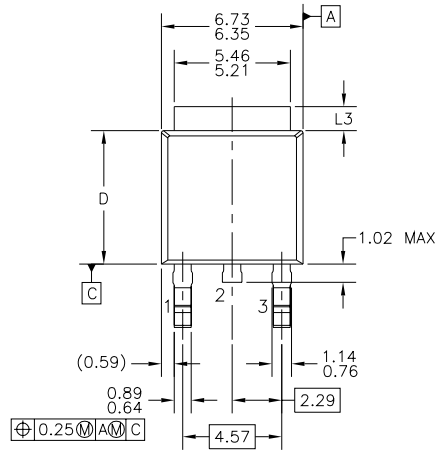


Peak Diode Recovery dv/dt Test Circuit & Waveforms

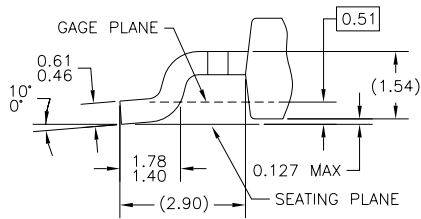
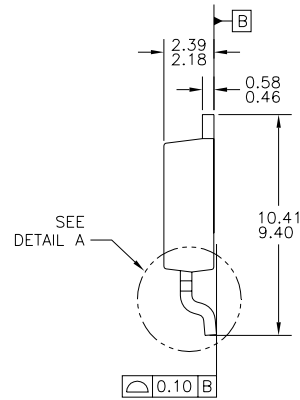
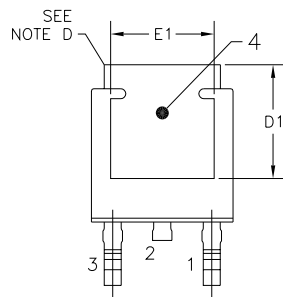


# Mechanical Dimensions

## D-PAK



LAND PATTERN RECOMMENDATION



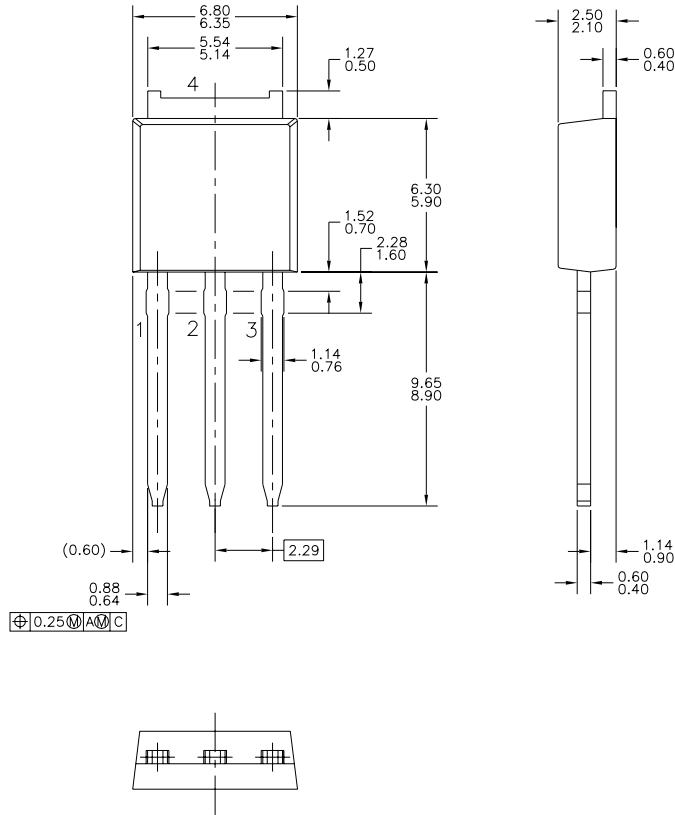
DETAIL A  
(ROTATED -90°)  
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:
- |    | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D  | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN  | 3.81 MIN  |
| D1 | 5.21 MIN  | 4.57 MIN  |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

Package Dimensions (Continued)

I-PAK



Dimensions in Millimeters



**TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT Quiet Series™	OCX™	SILENT SWITCHER®	UniFET™
ActiveArray™	GlobalOptoisolator™	OCXPro™	SMART START™	UltraFET®
Bottomless™	GTO™	OPTOLOGIC®	SPM™	VCX™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	Wire™
CoolFET™	I <sup>2</sup> C™	PACMAN™	SuperFET™	
CROSSVOLT™	i-Lo™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E <sup>2</sup> CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT™	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC™	
Programmable Active Droop™				

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I20