

# FCP7N60/FCPF7N60/FCPF7N60YDTU

## Features

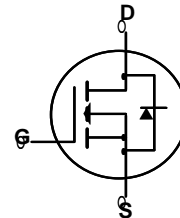
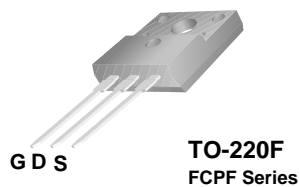
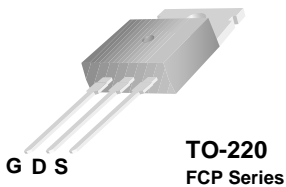
- 650V @T<sub>J</sub> = 150°C
- Typ. R<sub>ds(on)</sub>=0.53Ω
- Ultra low gate charge (typ. Q<sub>g</sub>=25nC)
- Low effective output capacitance (typ. C<sub>oss,eff</sub>=60pF)
- 100% avalanche tested
- RoHS Compliant



## Description

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



## Absolute Maximum Ratings

Symbol	Parameter	FCP7N60	FCPF7N60	Unit
V <sub>DSS</sub>	Drain-Source Voltage	600		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	7	7*	A
		4.4	4.4*	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	21	21*	A
V <sub>GSS</sub>	Gate-Source voltage	± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	230		mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	7		A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	8.3		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	83	31	W
		0.67	0.25	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		°C

\*Drain current limited by maximum junction temperature

## Thermal Characteristics

Symbol	Parameter	FCP7N60	FCPF7N60	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	1.5	4.0	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCP7N60	FCP7N60	TO-220	-	-	50
FCPF7N60	FCPF7N60	TO-220F	-	-	50
FCPF7N60	FCPF7N60YDTU	TO-220F (Forming)	-	-	50

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A, T_J = 25^\circ\text{C}$	600	--	--	V
		$V_{GS} = 0V, I_D = 250\mu A, T_J = 150^\circ\text{C}$	--	650	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$ , Referenced to $25^\circ\text{C}$	--	0.6	--	V/ $^\circ\text{C}$
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0V, I_D = 7A$	--	700	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	--	--	1	$\mu A$
		$V_{DS} = 480V, T_C = 125^\circ\text{C}$	--	--	10	$\mu A$
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	$V_{GS} = 30V, V_{DS} = 0V$	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -30V, V_{DS} = 0V$	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 3.5A$	--	0.53	0.6	$\Omega$
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40V, I_D = 3.5A$	--	6	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	--	710	920	pF
C <sub>oss</sub>	Output Capacitance		--	380	500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	34	--	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 480V, V_{GS} = 0V, f = 1.0\text{MHz}$	--	22	29	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	$V_{DS} = 0V$ to $400V, V_{GS} = 0V$	--	60	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 300V, I_D = 7A$ $R_G = 25\Omega$	--	35	80	ns
t <sub>r</sub>	Turn-On Rise Time		--	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	75	160	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	32	75
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 480V, I_D = 7A$ $V_{GS} = 10V$	--	23	30	nC
Q <sub>gs</sub>	Gate-Source Charge		--	4.2	5.5	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	11.5	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	21	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 7A$	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0V, I_S = 7A$ $di_F/dt = 100A/\mu s$	--	360	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	4.5	--	$\mu C$

**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 3.5A, V_{DD} = 50V, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 7A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

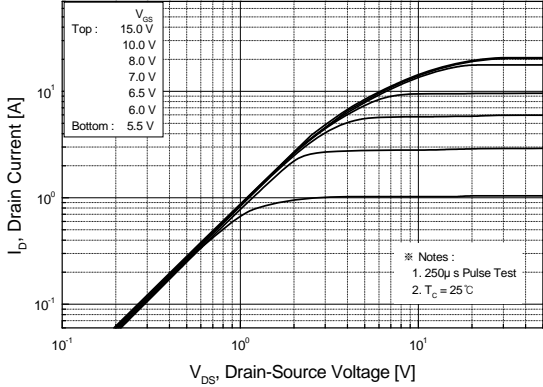


Figure 2. Transfer Characteristics

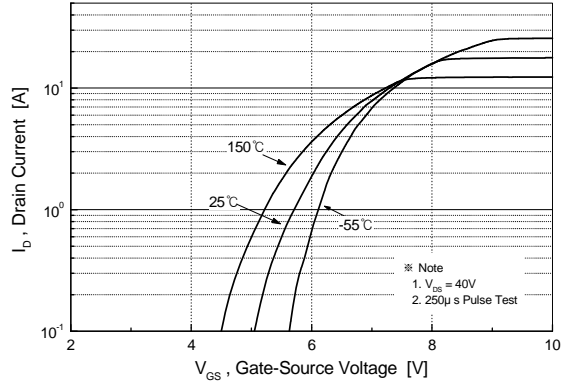


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

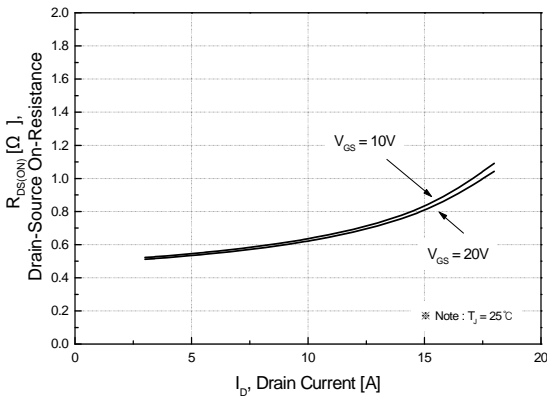


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

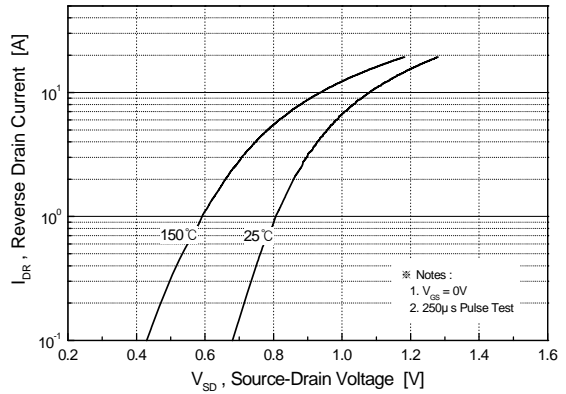


Figure 5. Capacitance Characteristics

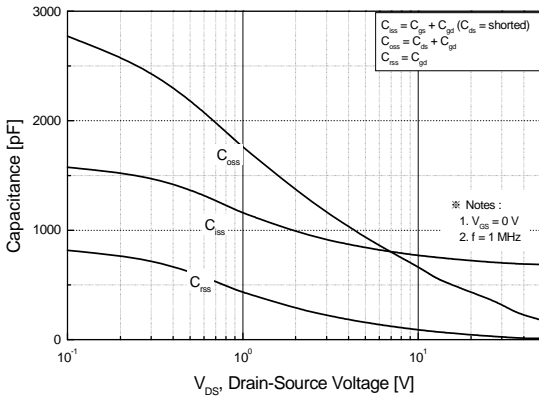
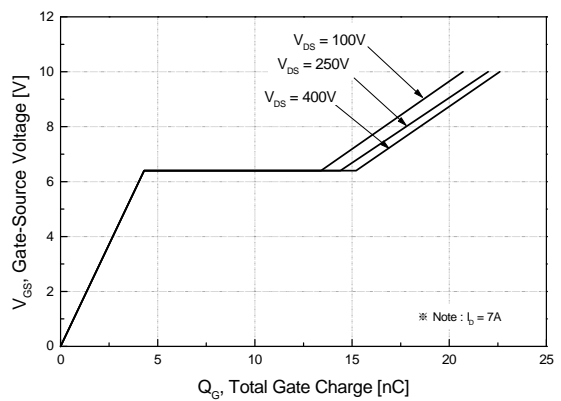


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

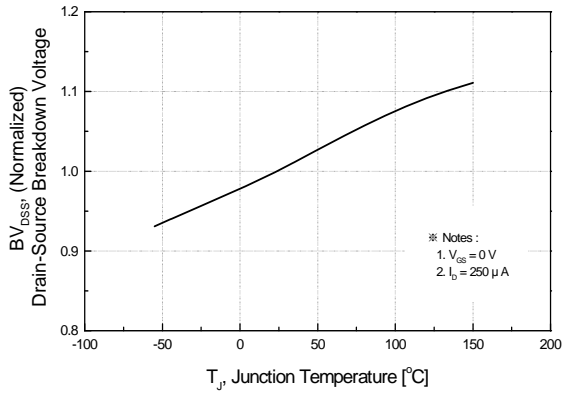


Figure 8. On-Resistance Variation vs. Temperature

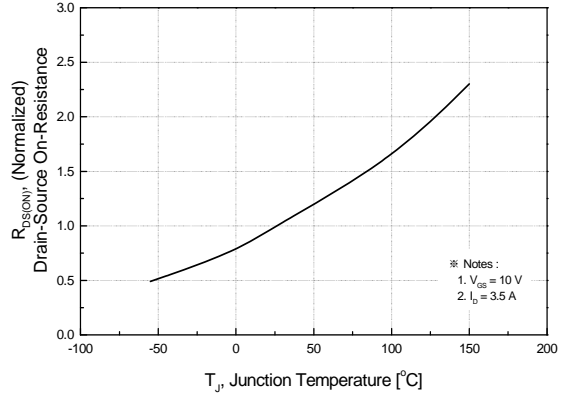


Figure 9-1. Maximum Safe Operating Area for FCP7N60

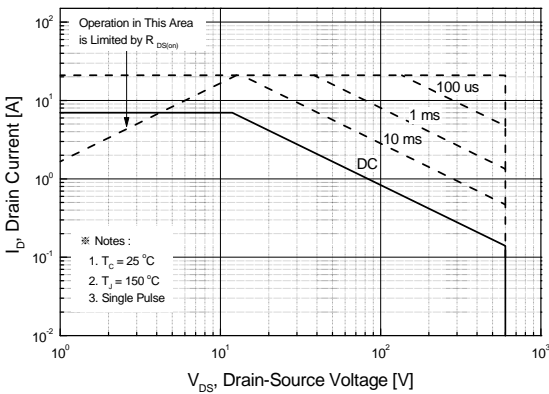


Figure 9-2. Maximum Safe Operating Area for FCPF7N60

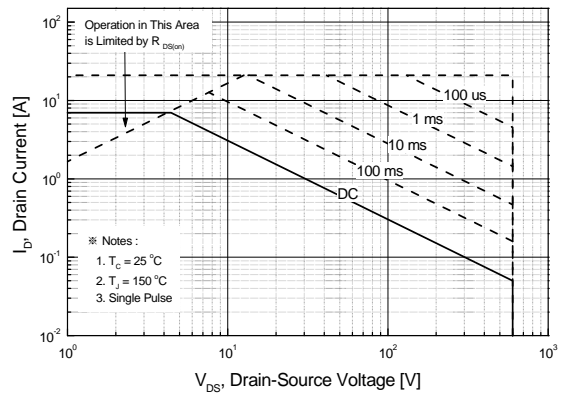
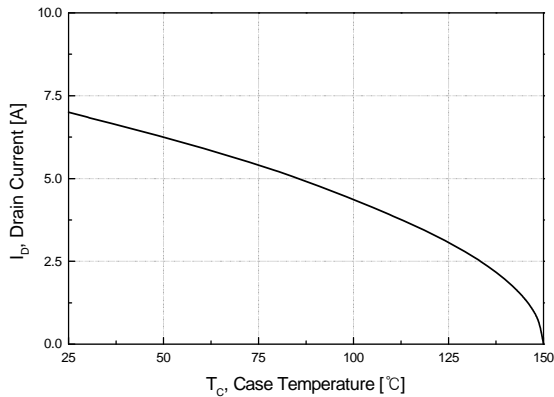


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve for FCP7N60

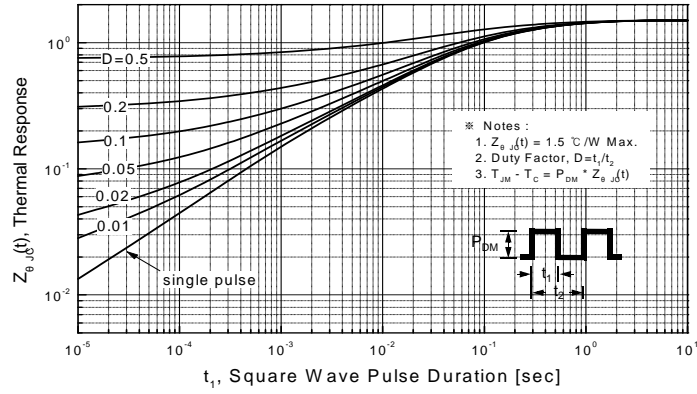
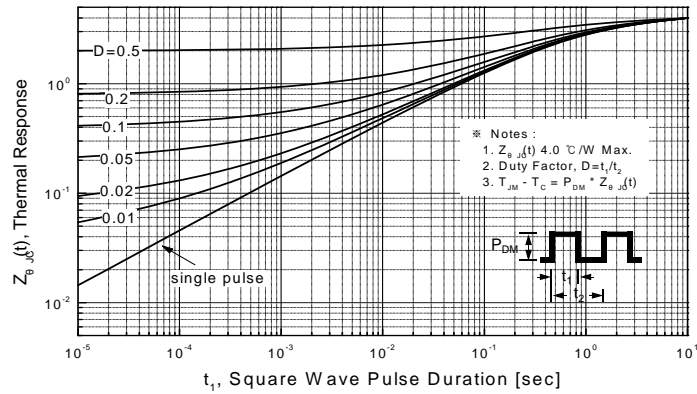
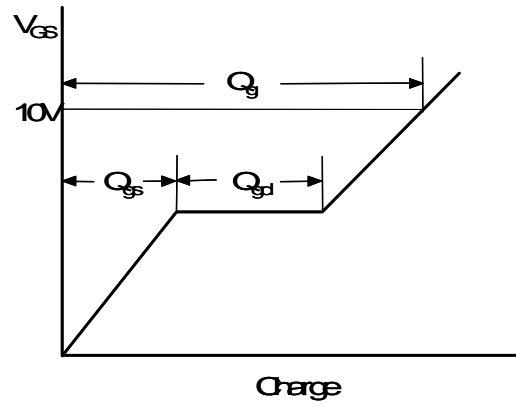
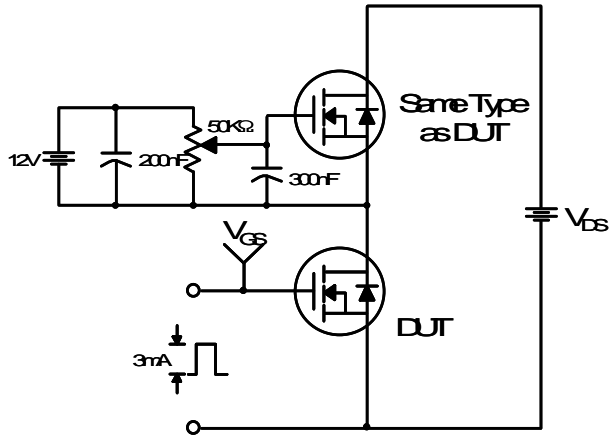


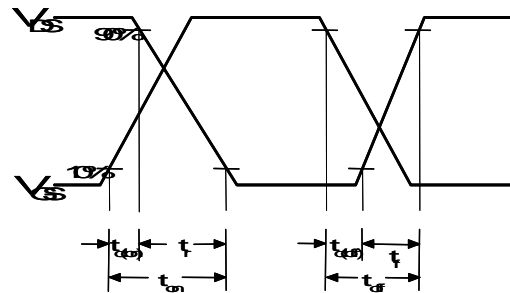
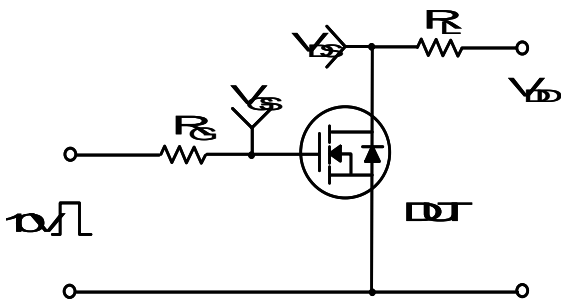
Figure 11-2. Transient Thermal Response Curve for FCPF7N60



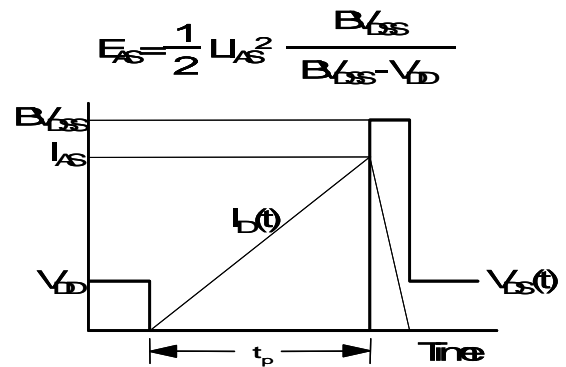
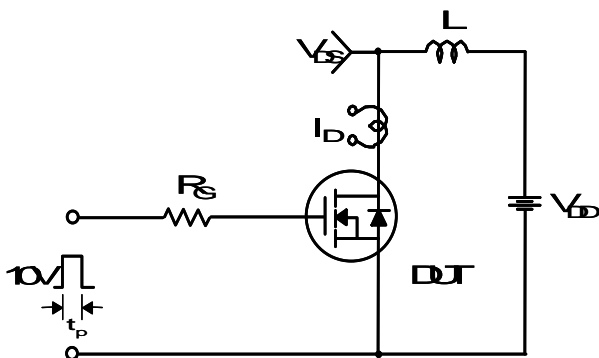
Gate Charge Test Circuit & Waveform



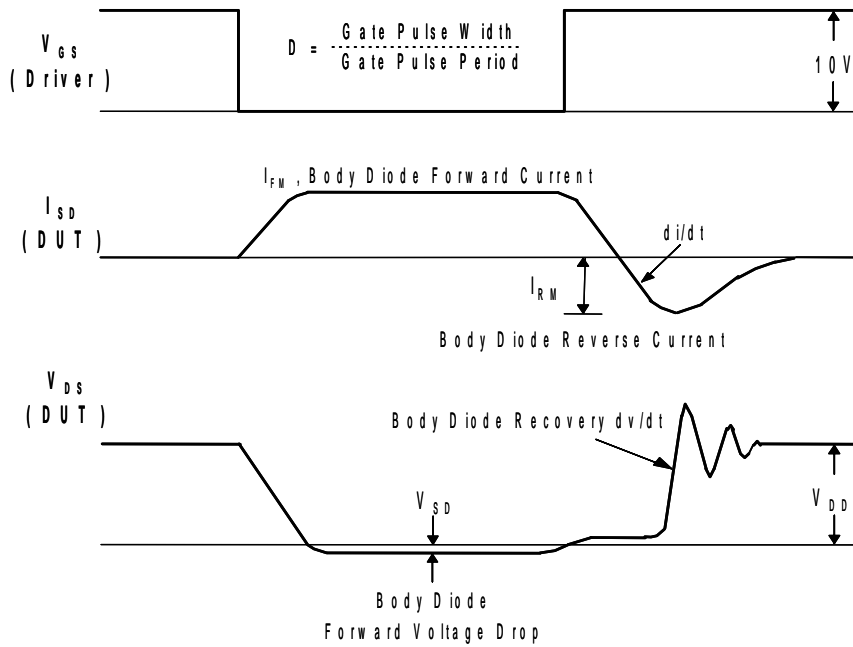
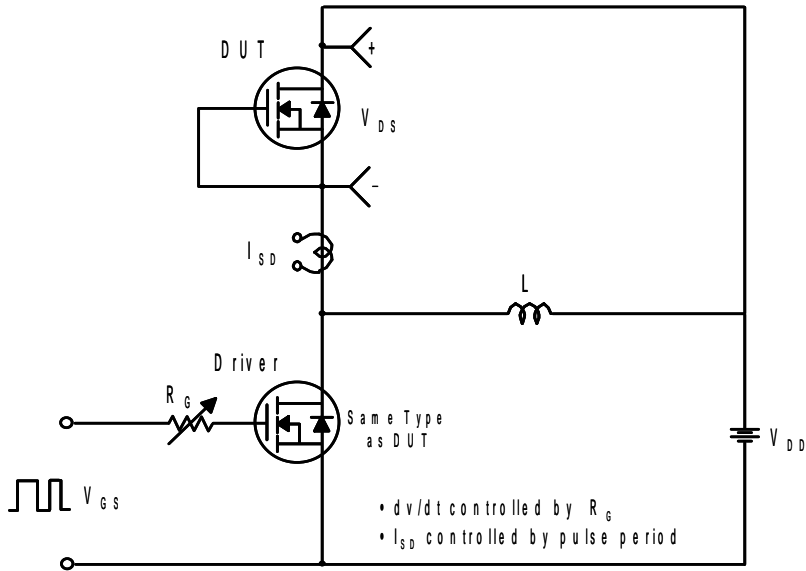
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

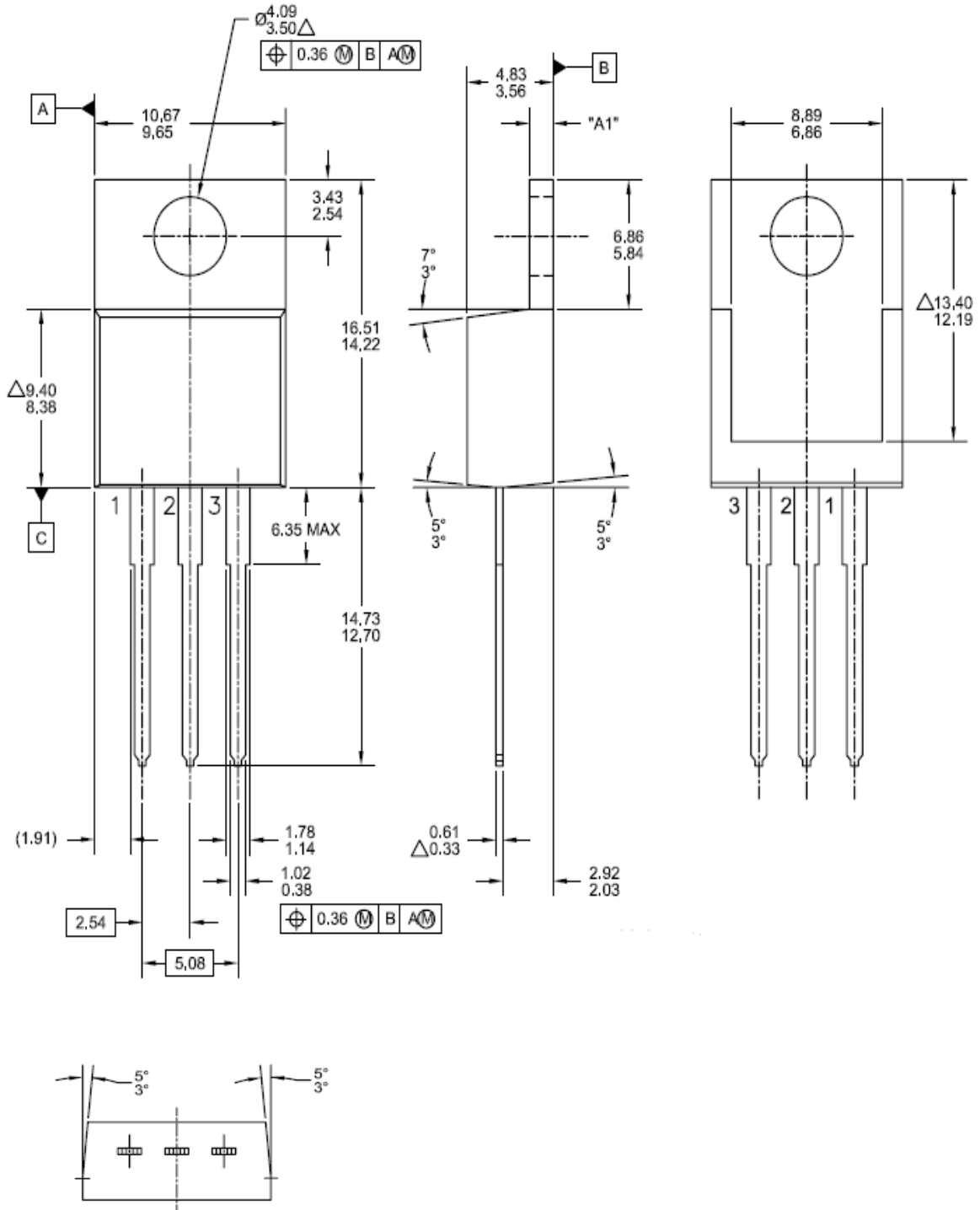


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO - 220

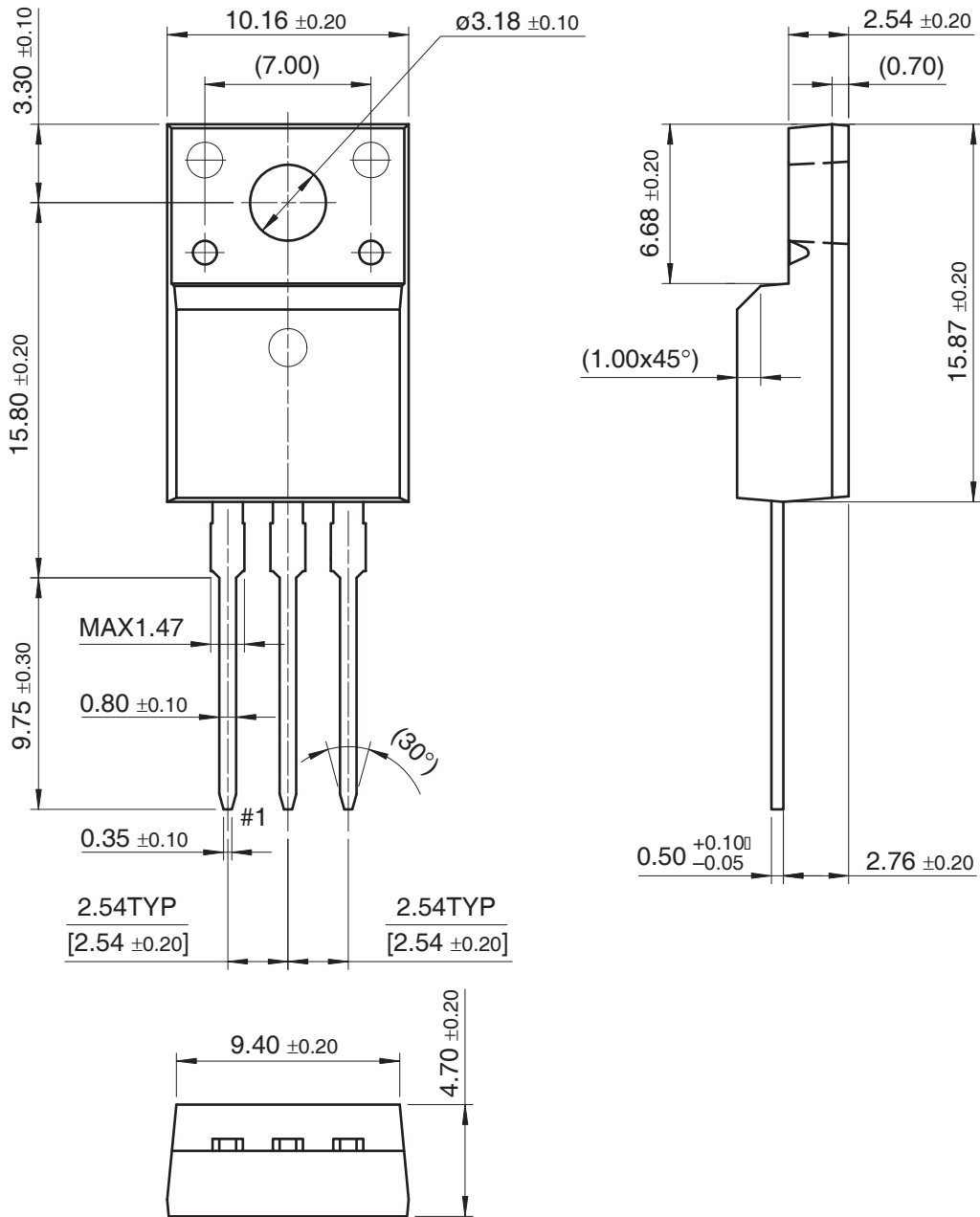


Dimensions in Millimeters



Mechanical Dimensions (Continued)

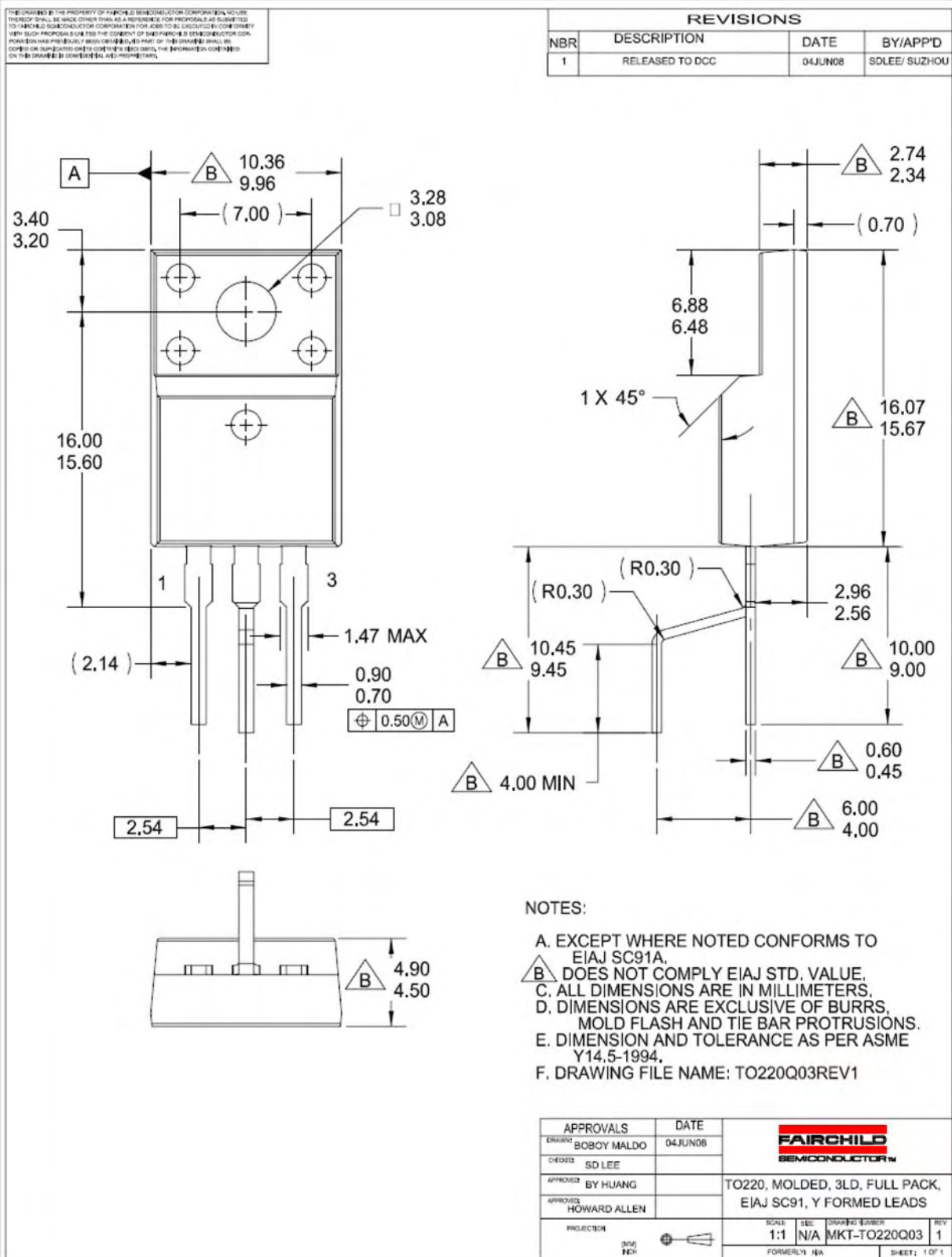
TO-220F



Dimensions in Millimeters

Mechanical Dimensions (Continued)

TO-220F (Y Forming)



**NOTES:**

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.

B. DOES NOT COMPLY EIAJ STD. VALUE.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.

F. DRAWING FILE NAME: TO220Q03REV1



APPROVALS	DATE	
DESIGNED: BOBOY MALDO	04JUN08	
CHECKED: SD LEE		
APPROVED: BY HUANG		
APPROVED: HOWARD ALLEN		TO220, MOLDED, 3LD, FULL PACK, EIAJ SC91, Y FORMED LEADS

PROJECTION	SCALE	REV
	1:1	1
	N/A	MKT-TO220Q03
	FORMERLY N/A	SHEET: 1 OF 1



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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