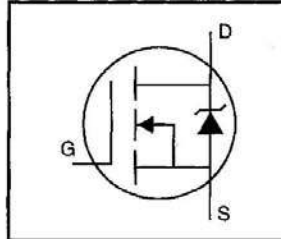


# IRFI720GPbF

## HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance
- Lead-Free

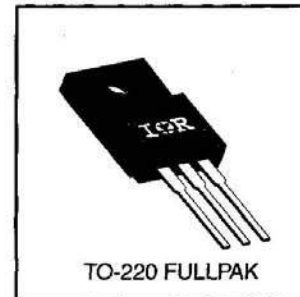


$V_{DSS} = 400V$
$R_{DS(on)} = 1.8\Omega$
$I_D = 2.6A$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.6	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	1.7	
$I_{DM}$	Pulsed Drain Current ①	10	
$P_D @ T_C = 25^\circ C$	Power Dissipation	30	W
	Linear Derating Factor	0.24	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy ②	150	mJ
$I_{AR}$	Avalanche Current ①	2.6	A
$E_{AR}$	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
$T_J$	Operating Junction and	-55 to +150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

### Thermal Resistance

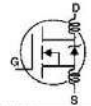
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

11/14/03

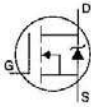
# IRFI720GPbF

International  
IR Rectifier

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

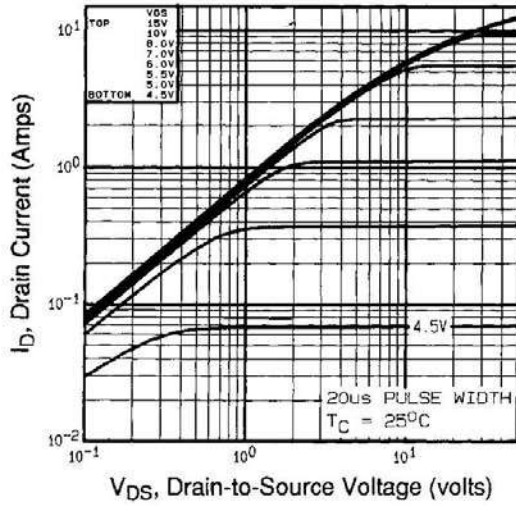
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.51	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.8	$\Omega$	$V_{GS}=10V, I_D=1.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	1.5	—	—	S	$V_{DS}=50V, I_D=1.6A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS}=400V, V_{GS}=0V$
		—	—	250		$V_{DS}=320V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
$Q_g$	Total Gate Charge	—	—	20	nC	$I_D=3.3A$
$Q_{gs}$	Gate-to-Source Charge	—	—	3.3		$V_{DS}=320V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	11		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—		$V_{DD}=200V$
$t_r$	Rise Time	—	14	—	ns	$I_D=3.3A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G=18\Omega$
$t_f$	Fall Time	—	13	—		$R_D=56\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	410	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	120	—		$V_{DS}=25V$
$C_{rss}$	Reverse Transfer Capacitance	—	47	—		$f=1.0\text{MHz}$ See Figure 5
C	Drain to Sink Capacitance	—	12	—		$f=1.0\text{MHz}$

## Source-Drain Ratings and Characteristics

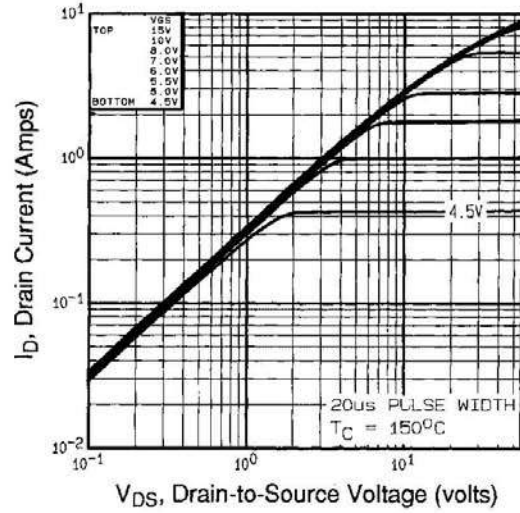
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	2.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	10		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}, I_S=2.6A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	300	600	ns	$T_J=25^\circ\text{C}, I_F=3.3A$
$Q_{rr}$	Reverse Recovery Charge	—	1.5	3.0	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

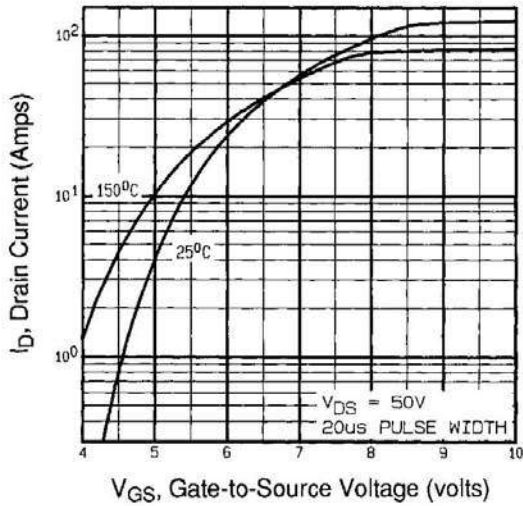
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=50V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=38\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=2.6A$  (See Figure 12)
- ③  $I_{SD}\leq 3.3A$ ,  $di/dt\leq 65A/\mu s$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$
- ⑤  $t=60s$ ,  $f=60\text{Hz}$



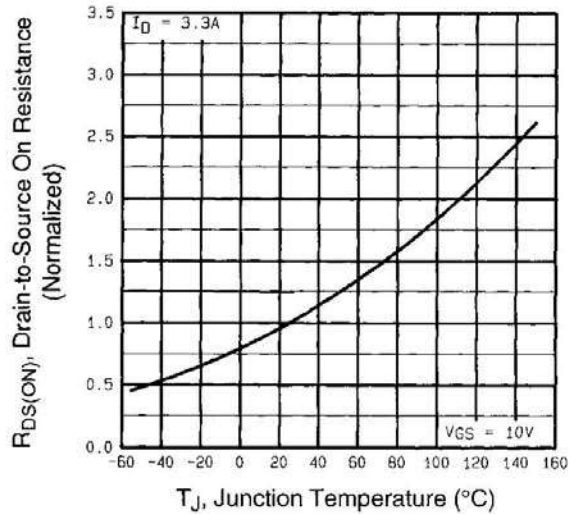
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$



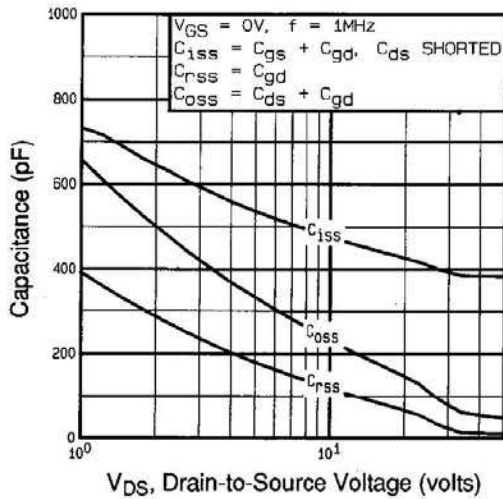
**Fig 3.** Typical Transfer Characteristics



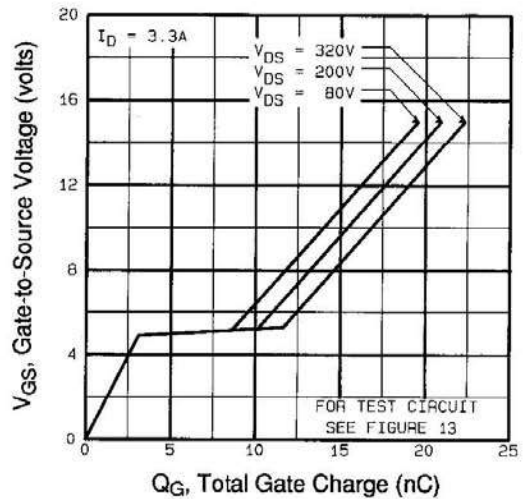
**Fig 4.** Normalized On-Resistance  
 Vs. Temperature

# IRFI720GPbF

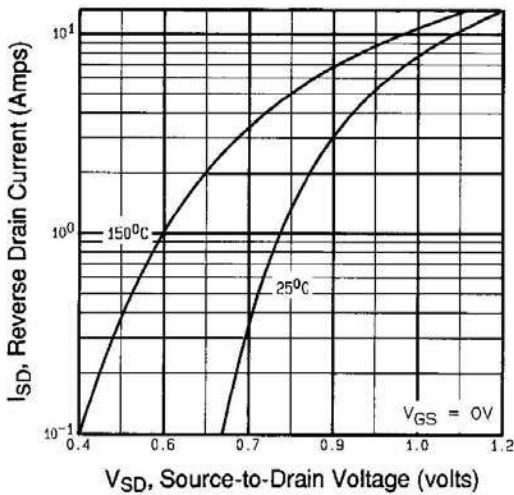
International  
IR Rectifier



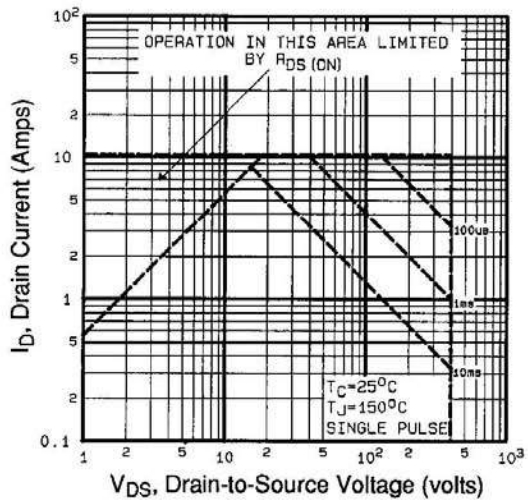
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



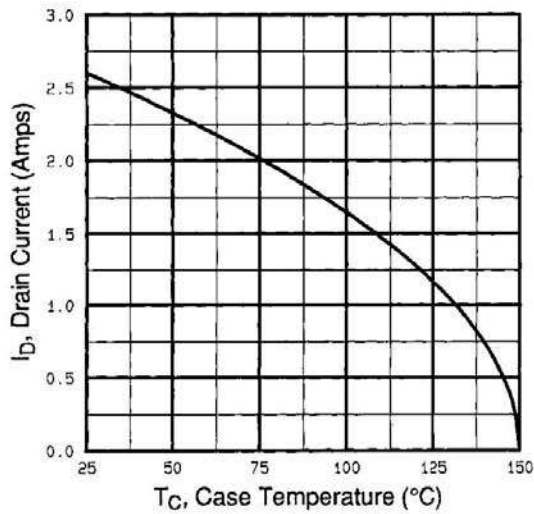
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



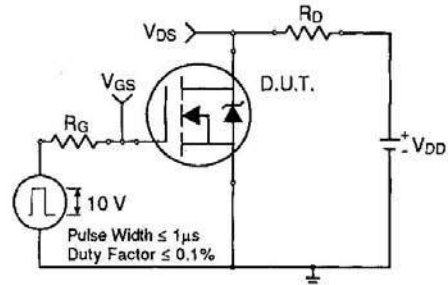
**Fig 7.** Typical Source-Drain Diode Forward Voltage



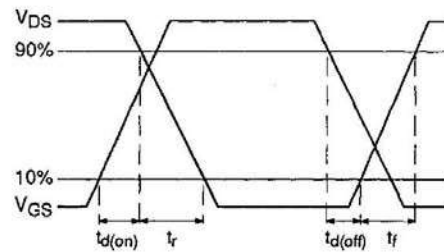
**Fig 8.** Maximum Safe Operating Area



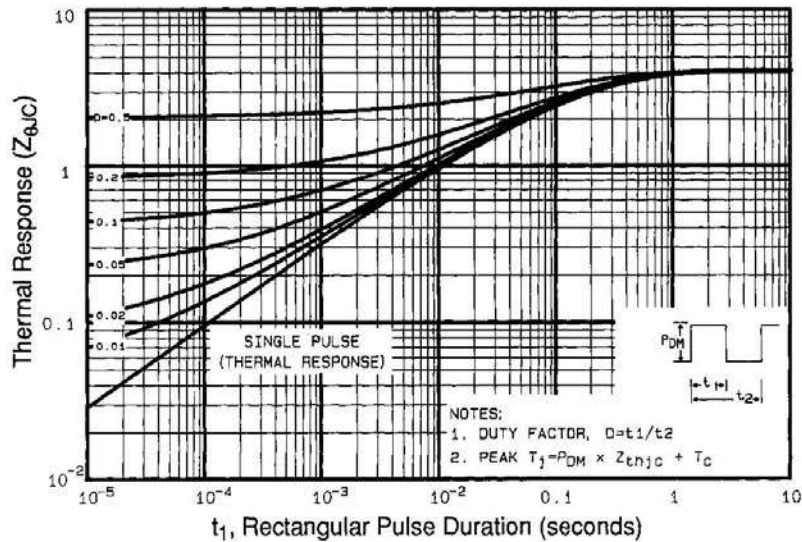
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



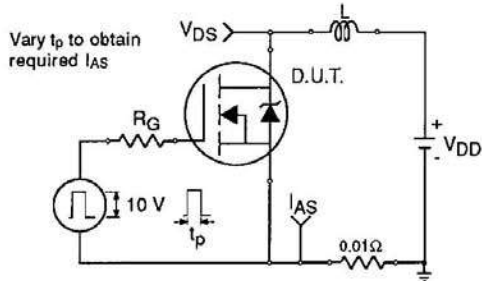
**Fig 10b.** Switching Time Waveforms



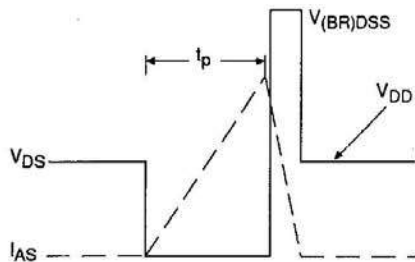
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRFI720GPbF

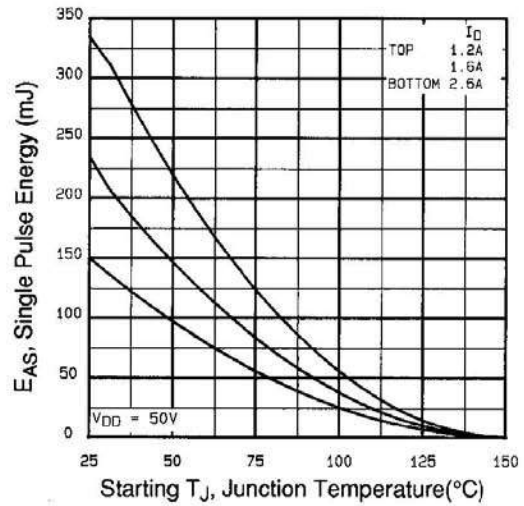
International  
**IR** Rectifier



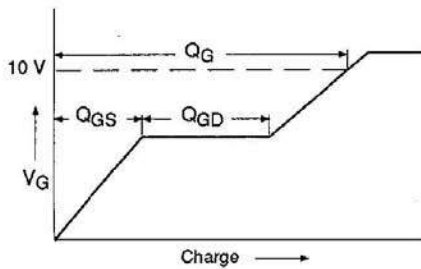
**Fig 12a.** Unclamped Inductive Test Circuit



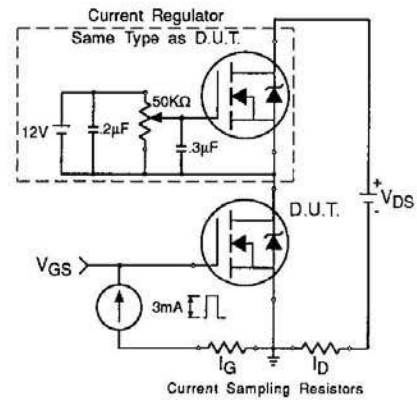
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



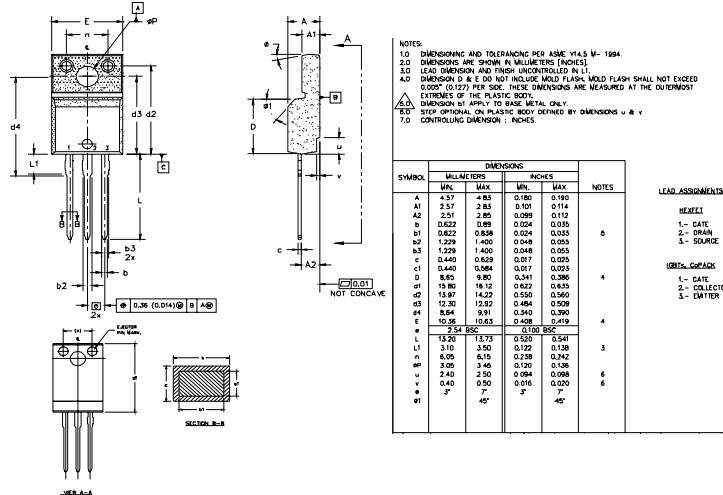
**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

## TO-220 Full-Pak Package Outline

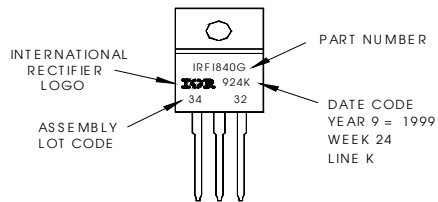
Dimensions are shown in millimeters (inches)



## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24 1999  
IN THE ASSEMBLY LINE "K"

**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



## Notice

The products described herein were acquired by Vishay Intertechnology, Inc., as part of its acquisition of International Rectifier's Power Control Systems (PCS) business, which closed in April 2007. Specifications of the products displayed herein are pending review by Vishay and are subject to the terms and conditions shown below.

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.

International Rectifier®, IR®, the IR logo, HEXFET®, HEXSense®, HEXDIP®, DOL®, INTERO®, and POWIRTRAIN® are registered trademarks of International Rectifier Corporation in the U.S. and other countries. All other product names noted herein may be trademarks of their respective owners.