NUS2401SNT1

Integrated PNP/NPN Digital Transistors Array

This new option of integrated digital transistors is designed to replace a discrete solution array of three transistors and their external resistor bias network. BRTs (Bias Resistor Transistors) contain a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT technology eliminates these individual components by integrating them into a single device, therefore the integration of three BRTs results in a significant reduction of both system cost and board space. This new device is packaged in the SC−74/Case 318F package which is designed for low power surface mount applications.

Features

- Integrated Design
- Reduces Board Space and Components Count
- Simplifies Circuitry Design
- Offered in Surface Mount Package Technology (SC−74)
- Available in 3000 Unit Tape and Reel
- Pb−Free Package is Available

Typical Applications

- Audio Muting Applications
- Drive Circuits Applications
- Industrial: Small Appliances, Security Systems, Automated Test
- Consumer: TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders

MAXIMUM RATINGS (Maximum Ratings are those values beyond which damage to the device may occur. Electrical Characteristics are not guaranteed over this range.)

Rating	Symbol	Value	Unit
Collector−Base Voltage	$V_{(BR)CBO}$	60	Vdc
Collector−Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter−Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current − Continuous	I_C	200	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation	P_D	350	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

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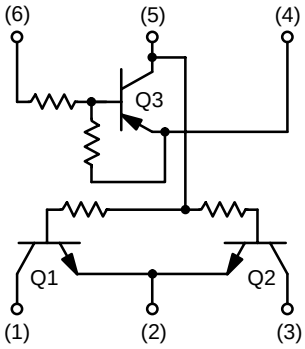
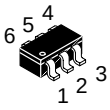
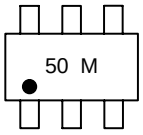




SC−74
CASE 318F
STYLE 4

MARKING DIAGRAM



50 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NUS2401SNT1	SC−74	3000/Tape & Reel
NUS2401SNT1G	SC−74 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

April, 2004 − Rev. 2

Publication Order Number:
NUS2401SNT1/D

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: T_J = 25°C for typical values, common for Q1, Q2, and Q3, − minus signed for Q3 (PNP) omitted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current (V_{CE} = 6.0 V, I_C = 0)	Q3 Q1, Q2	I_{EBO}	− −	− −	500 0.1	μA
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	V
Collector−Emitter Breakdown Voltage (Note 1) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	V
ON CHARACTERISTICS (Note 1)						
DC Current Gain	Q3 Q1, Q2	h_{FE}	35 150	60 350	− −	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA) (I_C = 10 mA, I_B = 1.0 mA)	 Q3 Q1, Q2	$V_{CE(sat)}$	 − −	 − −	 0.25 0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)		V_{OL}	−	−	0.2	V
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)		V_{OH}	4.9	−	−	V
Input Resistor	Q3 Q1, Q2	R1	7.0 0.13	10 0.175	13 0.22	kΩ
Resistor Ratio	Q3 Q1, Q2	R1/R2	− −	1.0 ∞	− −	

1. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2%.

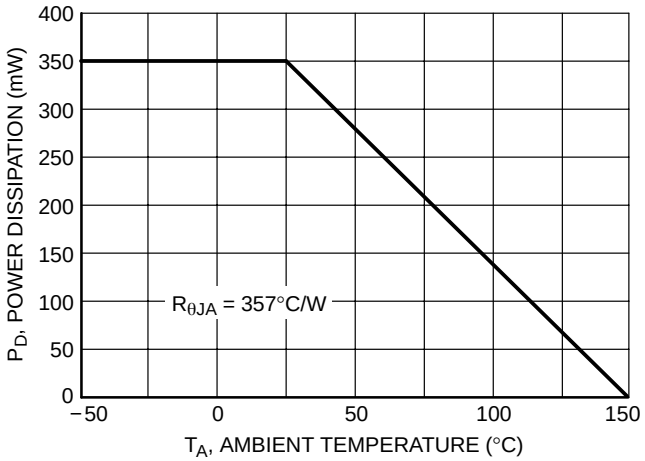


Figure 1. Derating Curve

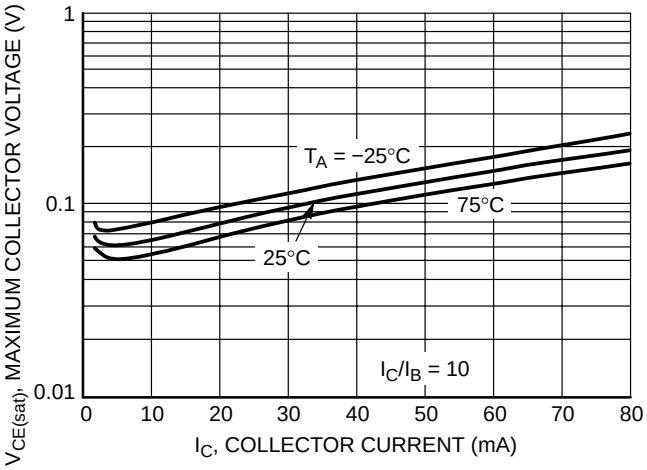


Figure 2. Maximum Collector Voltage versus Collector Current

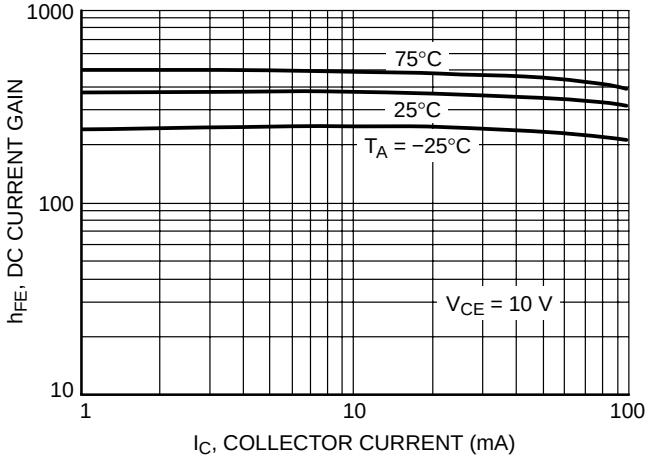


Figure 3. DC Current Gain

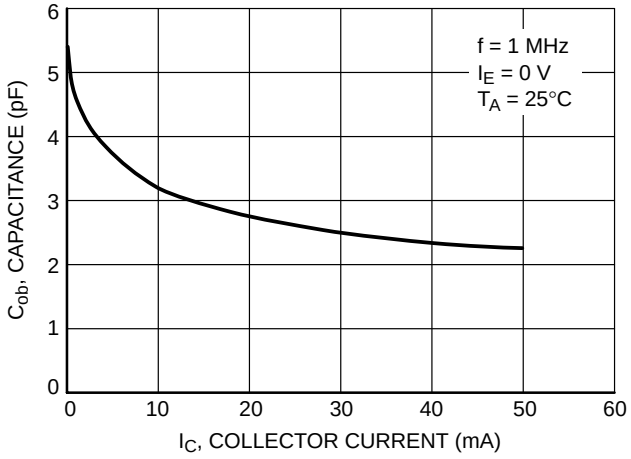


Figure 4. Output Capacitance

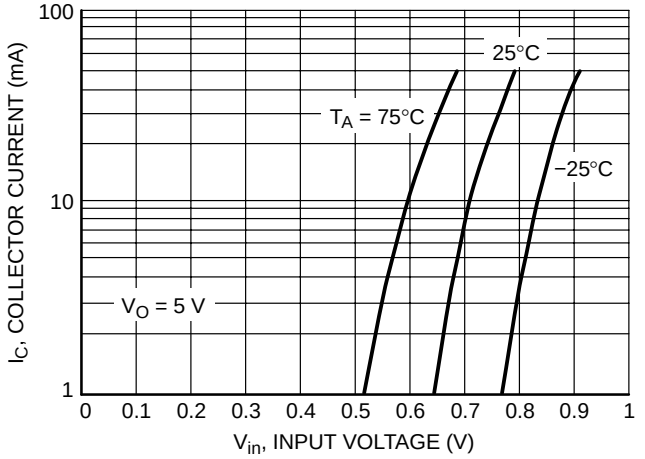


Figure 5. Output Current versus Input Voltage

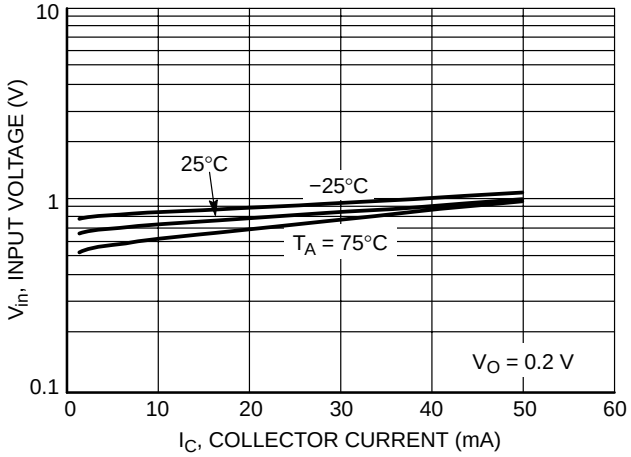


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − Q3 (PNP)

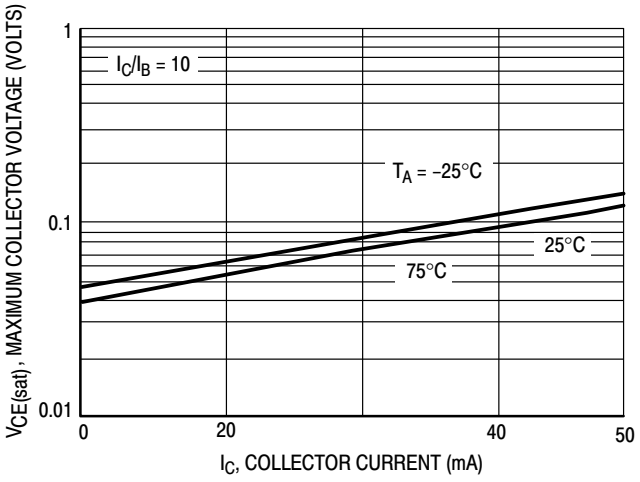


Figure 7. $V_{CE(sat)}$ versus I_C

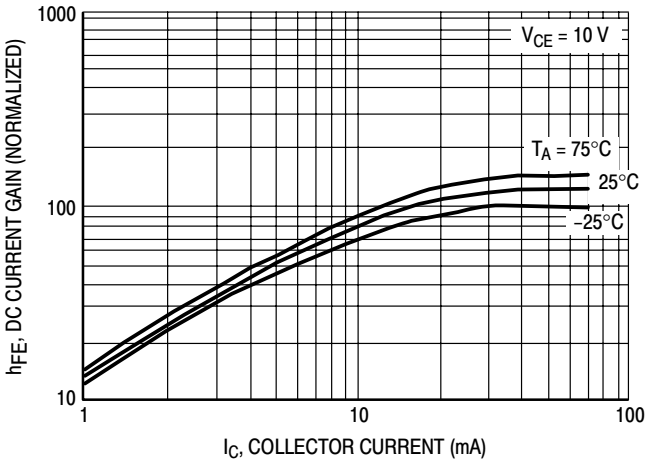


Figure 8. DC Current Gain

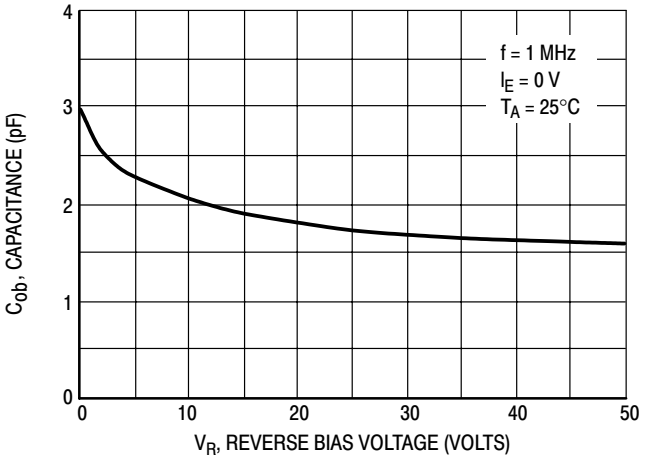


Figure 9. Output Capacitance

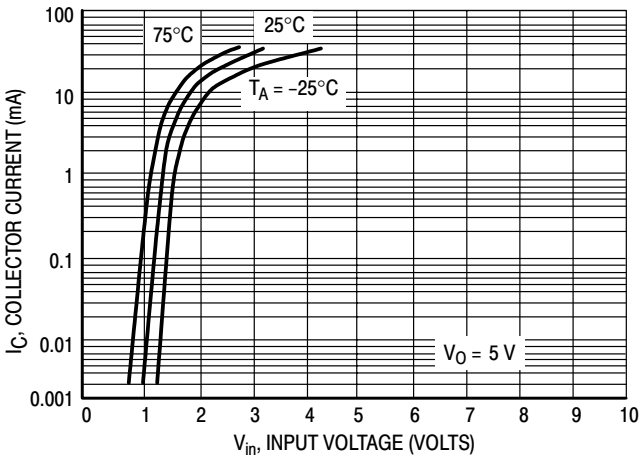


Figure 10. Output Current versus Input Voltage

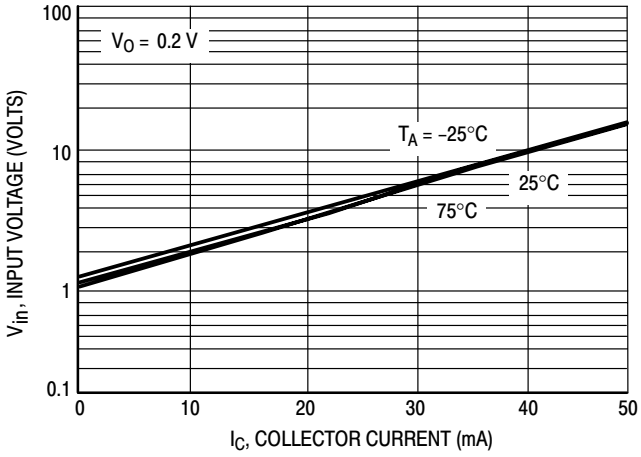
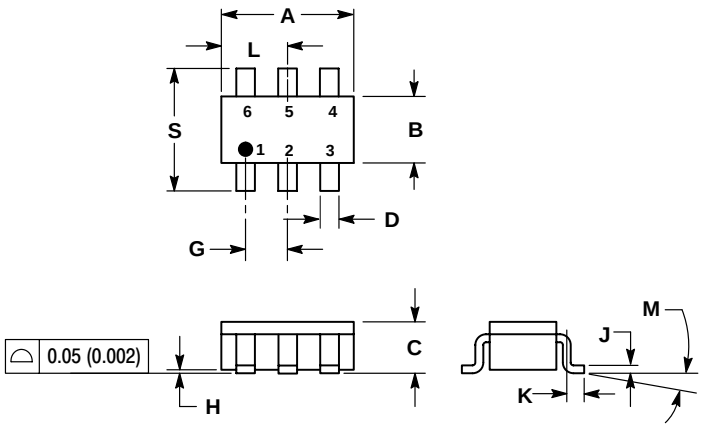


Figure 11. Input Voltage versus Output Current

PACKAGE DIMENSIONS

SC−74
CASE 318F−05
ISSUE K

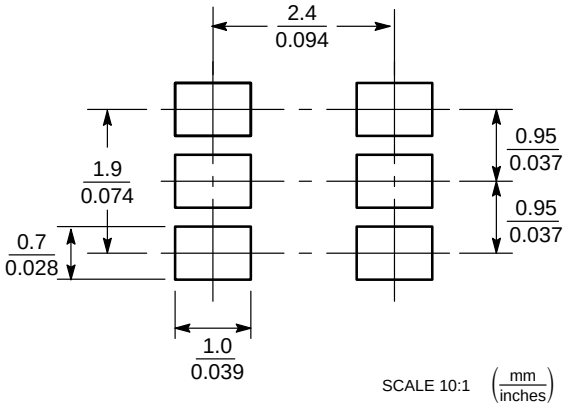


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03 OBSOLETE. NEW STANDARD 318F−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1142	0.1220	2.90	3.10
B	0.0512	0.0669	1.30	1.70
C	0.0354	0.0433	0.90	1.10
D	0.0098	0.0197	0.25	0.50
G	0.0335	0.0413	0.85	1.05
H	0.0005	0.0040	0.013	0.100
J	0.0040	0.0102	0.10	0.26
K	0.0079	0.0236	0.20	0.60
L	0.0493	0.0649	1.25	1.65
M	0 °	10 °	0 °	10 °
S	0.0985	0.1181	2.50	3.00

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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