ST16C2550

DUAL UART WITH 16-BYTE TRANSMIT AND RECEIVE FIFO'S

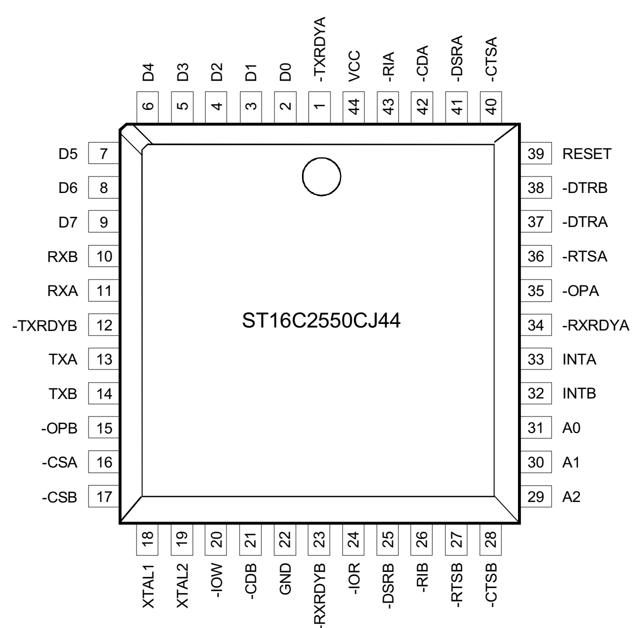
DESCRIPTION

The ST16C2550 (2550) is a dual universal asynchronous receiver and transmitter (UART). The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The 2550 provides enhanced UART functions with 16 byte FIFO's, a modem control interface, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loop-back capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50 Bps to 1.5 Mbps. The Baud rate generator can be configured for either crystal or external clock input. The 2550 is available in a 40-pin plastic-DIP, 44-pin PLCC, and 48-pin TQFP packages. The 40 pin package does not offer TXRDY and RXRDY pins (DMA Signal monitoring). Otherwise the three package versions are the same. The 2550 is functionally compatible with the 16C2450. The 2550 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Pin and functionally compatible to ST16C2450/ Software compatible with INS8250, NS16C550
- 1.5Mbps transmit/receive operation (24MHz Max.)
- 16 byte transmit FIFO to reduce the bandwidth requirement of the external CPU.
- 16 byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU.
- Independent transmit and receive UART control
- Four selectable Receive FIFO interrupt trigger levels
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD, and Software controllable line break)
- Programmable character lengths (5, 6, 7, 8) with Even, odd, or no parity
- Status report register
- Crystal or external clock input
- 460.8 Kbps transmit/receive operation with 7.3728 MHz crystal or external clock source
- TTL compatible inputs, outputs

PLCC Package



ORDERING INFORMATION

Part number	Pins	Package	Operating temperature
ST16C2550CP40	40	PDIP	0° C to + 70° C
ST16C2550CJ44	44	PLCC	0° C to + 70° C
ST16C2550CQ48	48	TQFP	0° C to + 70° C
ST16C2550IP40	40	PDIP	-40° C to + 85° C
ST16C2550IJ44	44	PLCC	-40° C to + 85° C
ST16C2550IQ48	48	TQFP	-40° C to + 85° C

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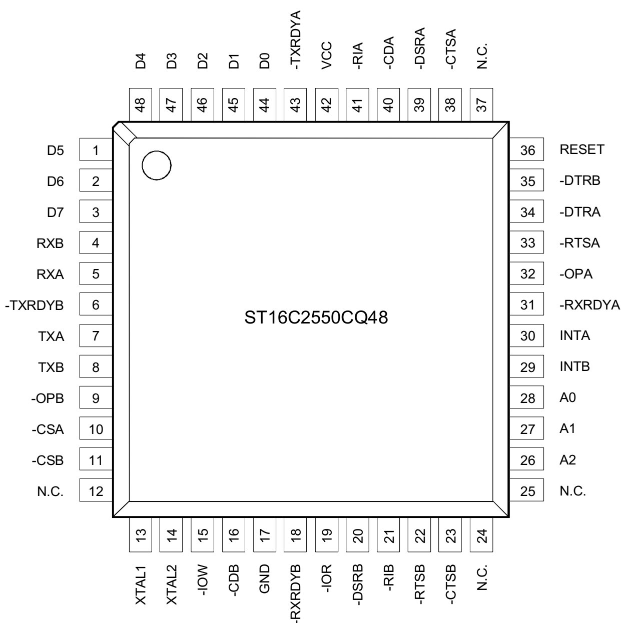
Figure 1, Package Descriptions, 40 pin, 48 pin ST16C2550

48 Pin TQFP Package



40 Pin DIP Package

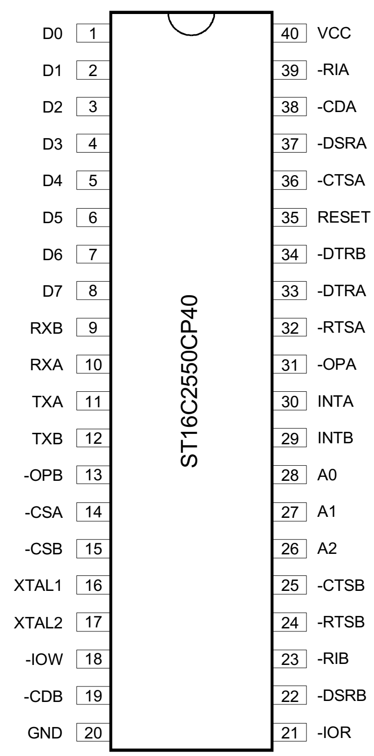
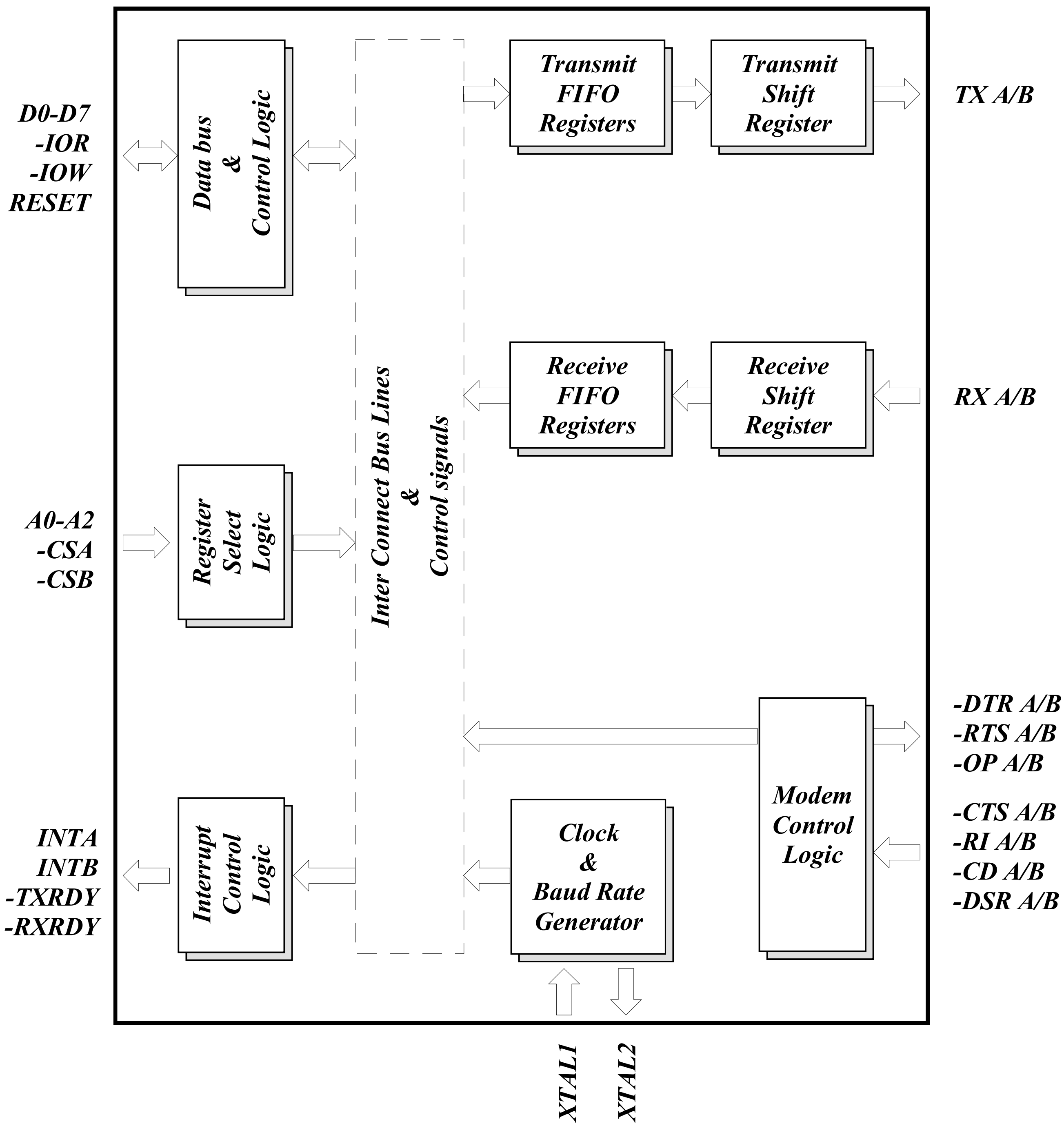


Figure 2, Block Diagram



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
A0	28	31	28	I	Address-0 Select Bit. - Internal register address selection.
A1	27	30	27	I	Address-1 Select Bit. - Internal register address selection.
A2	26	29	26	I	Address-2 Select Bit. - Internal register address selection.
-CS A-B	14,15	16,17	10,11	I	Chip Select A, B (active low) - This function is associated with individual channels, A through B. These pins enable data transfers between the user CPU and the 2550 for the channel(s) addressed. Individual UART sections (A, B) are addressed by providing a logic 0 on the respective -CS A-B pin.
D0-D7	1-8	2-9	44-48 1-3	I/O	Data Bus (Bi-directional) - These pins are the eight bit, three state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
GND	20	22	17	Pwr	Signal and power ground.
INT A-B	30,29	33,32	30,29	O	Interrupt A, B (three state) - This function is associated with individual channel interrupts, INT A-B. INT A-B are enabled when MCR bit-3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected.
-IOR	21	24	19	I	Read strobe. (active low Strobe) - A logic 0 transition on this pin will load the contents of an Internal register defined by address bits A0-A2 onto the 2550 data bus (D0-D7) for access by an external CPU.
-IOW	18	20	15	I	Write strobe. (active low strobe) - A logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0-A2.
-OP2 A-B	31,13	35,15	32,9	O	Output -2 (User Defined). - This function is associated with

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
					individual channels, A through B. The state at these pin(s) are defined by the user and through the software setting of MCR register bit-3. INT A-B are set to the active mode and OP2 to a logic 0 when MCR-3 is set to a logic 1. INT A-B are set to the three state mode and OP2 to a logic 1 when MCR-3 is set to a logic 0. See bit-3, Modem Control Register (MCR bit-3).
RESET	35	39	36	I	Reset. (active high) - A logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C2550 External Reset Conditions for initialization details.)
-RXRDY A-B	-	34,23	31,18	O	Receive Ready A-B (active low) - This function is associated with 44 pin PLCC and 48 pin TQFP packages only. This function provides the RX FIFO/RHR status for individual receive channels (A-B). RXRDY is primarily intended for monitoring DMA mode 1 transfers for the receive data FIFO's. A logic 0 indicates there is receive data to read/ unload, i.e., receive ready status with one or more RX characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been reached. This signal can also be used for single mode transfers (DMA mode 0).
-TXRDY A-B	-	1,12	43,6	O	Transmit Ready A-B (active low) - This function is associated with 44 pin PLCC and 48 pin TQFP packages only. These outputs provide the TX FIFO/THR status for individual transmit channels (A-B). TXRDY is primarily intended for monitoring DMA mode 1 transfers for the transmit data FIFO's. An individual channel's -TXRDY A-B buffer ready status is indicated by logic 0, i.e., at least one location is empty and available in the FIFO or THR. This pin goes to a logic 1 when there are no more empty locations in the FIFO or THR. This signal can also be used for single mode transfers (DMA mode 0).
VCC	40	44	42	Pwr	Power supply input.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
XTAL1	16	18	13	I	Crystal or External Clock Input - Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. This configuration requires an external 1 MW resistor between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to this pin to provide custom data rates (see Baud Rate Generator Programming).
XTAL2	17	19	14	O	Output of the Crystal Oscillator or Buffered Clock - (See also XTAL1). Crystal oscillator output or buffered clock output. Should be left open if an external clock is connected to XTAL1.
-CD A-B	38,19	42,21	40,16	I	Carrier Detect (active low) - These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
-CTS A-B	36,25	40,28	38,23	I	Clear to Send (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on the -CTS pin indicates the modem or data set is ready to accept transmit data from the 2550. Status can be tested by reading MSR bit-4. This pin has no effect on the UART's transmit or receive operation.
-DSR A-B	37,22	41,25	39,20	I	Data Set Ready (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
-DTR A-B	33,34	37,38	34,35	O	Data Terminal Ready (active low) - These outputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates that the 2550 is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0, or after a reset. This

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
					pin has no effect on the UART's transmit or receive operation.
-RI A-B	39,23	43,26	41,21	I	Ring Indicator (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
-RTS A-B	32,24	36,27	33,22	O	Request to Send (active low) - These outputs are associated with individual UART channels, A through B. A logic 0 on the -RTS pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin has no effect on the UART's transmit or receive operation.
RX A-B	10,9	11,10	5,4	I	Receive Data (A-B) - These inputs are associated with individual serial channel data to the 2550 receive input circuits, A-B. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pin is disabled and TX data is connected to the UART RX Input, internally.
TX A-B	11,12	13,14	7,8	O	Transmit Data (A-B) - These outputs are associated with individual serial transmit channel data from the 2550. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX output pin is disabled and TX data is internally connected to the UART RX Input.

GENERAL DESCRIPTION

The 2550 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The 2550 represents such an integration with greatly enhanced features. The 2550 is fabricated with an advanced CMOS process.

The 2550 is an upward solution that provides a dual UART capability with 16 bytes of transmit and receive FIFO memory, instead of none in the 16C2450. The 2550 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 2550 by the transmit and receive FIFO's. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C2450 without a receive FIFO, will require unloading of the RHR in 93 microseconds (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO less than every 100 microseconds. However with the 16 byte FIFO in the 2550, the data buffer will not require unloading/loading for 1.53 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable receive FIFO trigger interrupt levels is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 2550 is capable of operation to 1.5Mbps with a 24 MHz. With a crystal or external clock input of 7.3728 MHz the user can select data rates up to 460.8 Kbps.

The rich feature set of the 2550 is available through internal registers. Selectable receive FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls are all standard features. Following a power on reset or an external reset, the 2550 is software compatible with the previous generation, ST16C2450.

FUNCTIONAL DESCRIPTIONS

UART A-B Functions

The UART provides the user with the capability to Bi-directionally transfer information between an external CPU, the 2550 package, and an external serial device. A logic 0 on chip select pins -CSA and/or -CSB allows the user to configure, send data, and/or receive data via UART channels A-B. Individual channel select functions are shown in Table 2 below.

Table 2, SERIAL PORT SELECTION GUIDE

CHIP SELECT	Function
-CS A-B = 1s	None
-CS A = 0	UART CHANNEL A
-CS B = 0	UART CHANNEL B

Internal Registers

The 2550 provides two sets of internal registers (A and B) consisting of 12 registers each for monitoring and controlling the functions of each channel of the UART. These resisters are shown in Table 3 below. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR).

Table 3, INTERNAL REGISTER DECODE

A2	A1	A0	READ MODE	WRITE MODE
General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR): Note 1*				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
Baud Rate Register Set (DLL/DLM): Note *2				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

Note 1* The General Register set is accessible only when CS A/B is a logic 0.
Note 2* The Baud Rate register set is accessible only when CS A/B is a logic 0 and LCR bit-7 is a logic 1.

FIFO Operation

The 16 byte transmit and receive data FIFO's are enabled by the FIFO Control Register (FCR) bit-0. The user can set the receive trigger level via FCR bits 6-7 but not the transmit trigger level. The transmit interrupt trigger level is set to 16 following a reset. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Hardware/Software and Time-out Interrupts

The interrupts are enabled by IER bits 0-3. Care must be taken when handling these interrupts. Following a reset the transmitter interrupt is enabled, the 2550 will issue an interrupt to indicate that transmit holding register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/ RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER bit-3). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case the 2550 FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should recheck LSR bit-0 for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read.. The actual time out value is T (**T**ime out length in bits) = 4 X P (**P**rogrammed word length) + 12. To convert the time out value to a character value, the user has to consider the complete word length, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1X, 1.5X, or 2X bit times.

Example -A: If the user programs a word length of 7, with no parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) +12 = 40 bit times. The character time will be equal to 40 / 9 = 4.4 characters, or as shown in the fully worked out example: T = [(programmed word length = 7) + (stop bit = 1) + (start bit = 1) = 9]. 40 (bit times divided by 9) = 4.4 characters.

Example -B: If the user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bit times. Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Programmable Baud Rate Generator

The 2550 supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The 2550 can support a standard data rate of 921.6Kbps.

Single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate. The 2550 can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/ 22-33 pF load) is connected externally between the XTAL1 and XTAL2 pins, with an external 1 MΩ resistor across it. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. (see Baud Rate Generator Programming).

The generator divides the input 16X clock by any divisor from 1 to 2^{16} -1. The 2550 divides the basic external clock by 16. The basic 16X clock provides table rates to support standard and custom applications using the same system design. The rate table is configured via the DLL and DLM internal register functions. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 4 below, shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

Crystal oscillator connection

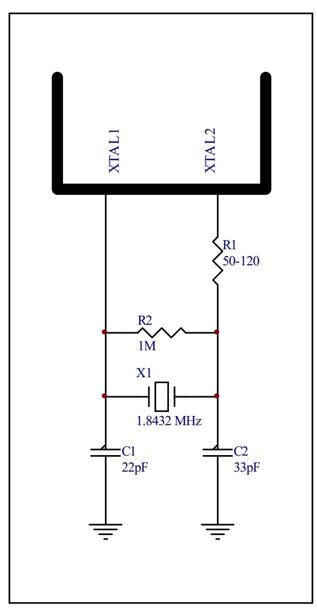


Table 4, BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

Output Baud Rate	Output 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	2304	900	09	00
75	1536	600	06	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
3600	32	20	00	20
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2k	6	06	00	06
38.4k	3	03	00	03
57.6k	2	02	00	02
115.2k	1	01	00	01

DMA Operation

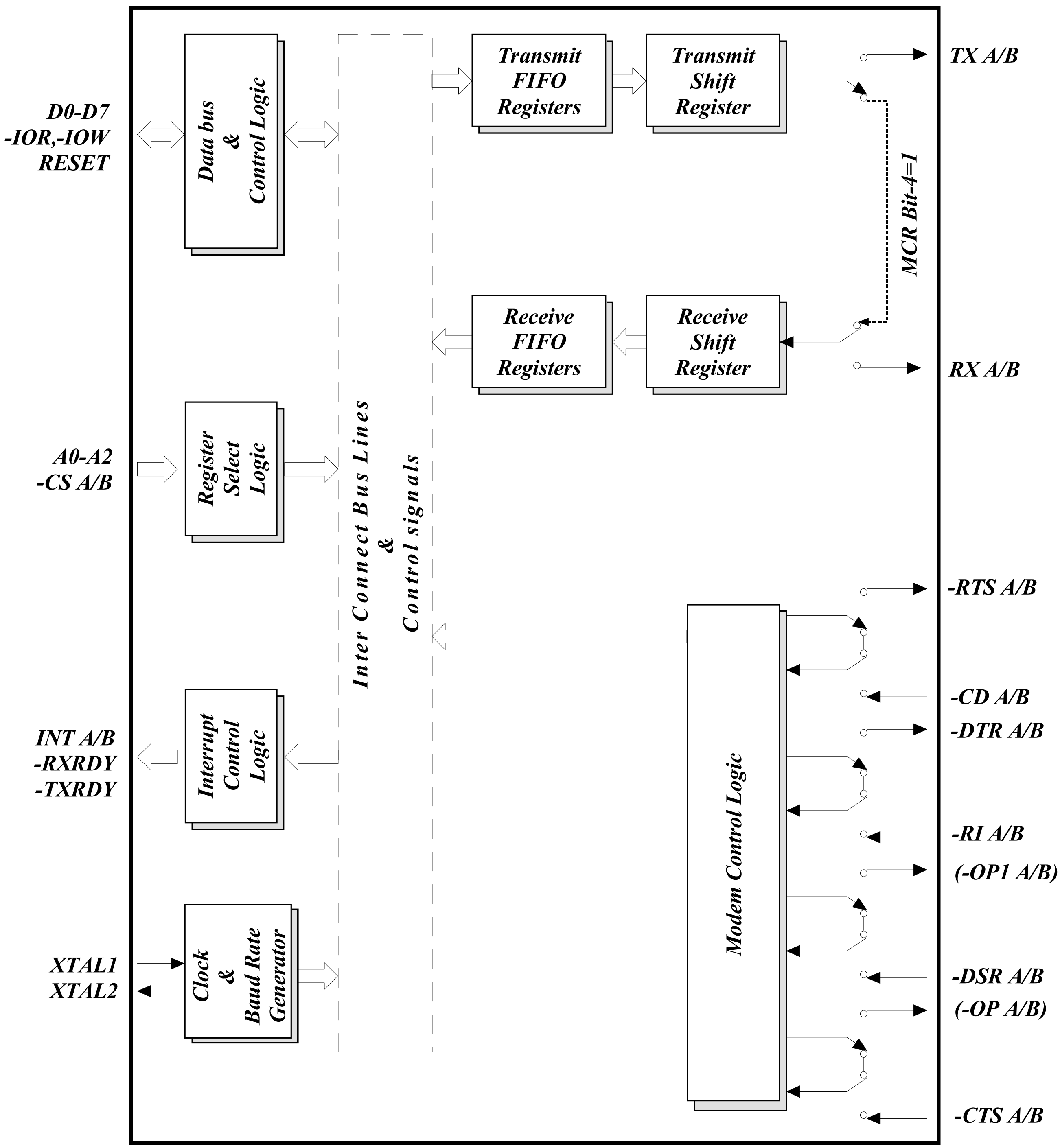
The 2550 FIFO trigger level provides additional flexibility to the user for block mode operation. LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFO's in the DMA mode (FCR bit-3). When the transmit and receive FIFO's are enabled and the DMA mode is deactivated (DMA Mode "0"), the 2550 activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode "1"), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the receive trigger level and the transmit FIFO. In this mode, the 2550 sets the interrupt output pin when characters in the transmit FIFO is below 16, or the characters in the receive FIFO's are above the receive trigger level.

Loop-back Mode

The internal loop-back capability allows onboard diagnostics. In the loop-back mode the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR register bits 0-3 are used for controlling loop-back diagnostic testing. In the loop-back mode INT enable and MCR bit-2 in the MCR register (bits 3/2) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 4). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -DTR, -RTS, INT enable and MCR bit-2. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Control Register (MCR bits 0-3) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.

Figure 4, INTERNAL LOOP-BACK MODE DIAGRAM



REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the twelve 2550 internal registers. The assigned bit functions are more fully defined in the following paragraphs.

Table 5, ST16C2550 INTERNAL REGISTERS

A2 A1 A0	Register [Default] Note 3*	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
General Register Set: Note 1*									
0 0 0	RHR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER [00]	0	0	0	0	Modem Status Interrupt	Receive Line Status interrupt	Transmit Holding Register interrupt	Receive Holding Register
0 1 0	FCR [00]	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR [01]	FIFO's enabled	FIFO's enabled	0	0	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR [00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR [00]	0	0	0	loop back	-OP2/ INT enable	-OP1	-RTS	-DTR
1 0 1	LSR [60]	FIFO data error	THR & TSR empty	THR. empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR [X0]	CD	RI	DSR	CTS	delta -CD	delta -RI	delta -DSR	delta -CTS
1 1 1	SPR [FF]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Special Register Set: Note *2									
0 0 0	DLL [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM [XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

Note 1* The General Register set is accessible only when CS A/B is a logic 0.
Note 2* The Baud Rate register set is accessible only when CS A/B is a logic 0 and LCR bit-7 is a logic 1.
Note 3* The value between the square brackets represents the register's initialized HEX value, X = N/A.

Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the TSR and UART via the THR, providing that the THR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = FIFO full, logic 1= at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register, RHR and a Receive Serial Shift Register (RSR). Receive data is removed from the 2550 and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT A-B output pins.

IER Vs Transmit/Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the receive interrupts and register status will reflect the following:

A) The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.

B) Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C) The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.

D) When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR register or by loading the THR with new data characters.

IER Vs Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1; resetting IER bits 0-3 enables the 2550 in the FIFO polled mode of operation. In this mode interrupts are not generated and the user must poll the LSR register for TX and/or RX data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A) LSR BIT-0 will be a logic 1 as long as there is one byte in the receive FIFO.

B) LSR BIT 1-4 will provide the type of receive errors, or a receive break, if encountered.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both the transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will show if any FIFO data errors occurred.

IER BIT-0:
In the 16C450 mode, This interrupt will be issued when the RHR has data or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level.
Logic 0 = Disable the receiver ready (ISR level 2, RXRDY) interrupt. (normal default condition)
Logic 1 = Enable the RXRDY (ISR level 2) interrupt.

IER BIT-1:
In the 16C450 mode, this interrupt will be issued whenever the THR is empty and is associated with bit-5 in the LSR register. In the FIFO modes, this interrupt will be issued whenever the FIFO and THR are empty
Logic 0 = Disable the Transmit Holding Register Empty (TXRDY) interrupt. (normal default condition)
Logic 1 = Enable the TXRDY (ISR level 3) interrupt.

IER BIT-2:
This interrupt will be issued whenever an receive data error condition exists as reflected in LSR bits 1-4.
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

IER BIT-3:
This interrupt will be issued whenever there is a modem status change as reflected in MSR bits 0-3.
Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

IER BIT 4-7:
Not Used - initialized to a logic 0.

FIFO Control Register (FCR)

This register is used to enable the FIFO's, clear the FIFO's, set the receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

DMA MODE
Mode 0 Set and enable the interrupt for each single transmit or receive operation, and is similar to the ST16C450 mode. Transmit Ready (-TXRDY) on 44/48 pin packages will go to a logic 0 when ever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready (-RXRDY) on 44,/48 pin packages will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.
Mode 1 Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is below the programmed trigger level. -TXRDY on 44/48 pin packages remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However the FIFO continues to fill regardless of the programmed level until the FIFO is full. -RXRDY on 44/48 pin packages remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

FCR BIT-0:
Logic 0 = Disable the transmit and receive FIFO. (normal default condition)
Logic 1 = Enable the transmit and receive FIFO. This bit must be a "1" when other FCR bits are written to or they will not be programmed.

FCR BIT-1:
Logic 0 = No FIFO receive reset. (normal default condition)
Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-2:
Logic 0 = No FIFO transmit reset. (normal default condition)
Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-3:
Logic 0 = Set DMA mode “0”. (normal default condition)
Logic 1 = Set DMA mode “1.”

Transmit operation in mode “0”:
When the 2550 is in the ST16C450 mode (FIFO’s disabled, FCR bit-0 = logic 0) or in the FIFO mode (FIFO’s enabled, FCR bit-0 = logic 1, FCR bit-3 = logic 0) and when there are no characters in the transmit FIFO or transmit holding register, the -TXRDY pin in 44/48 pin packages will be a logic 0. Once active the -TXRDY pin will go to a logic 1 after the first character is loaded into the transmit holding register.

Receive operation in mode “0”:
When the 2550 is in mode “0” (FCR bit-0 = logic 0) or in the FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 0) and there is at least one character in the receive FIFO, the -RXRDY pin will be a logic 0. Once active the -RXRDY pin on 44/48 pin packages will go to a logic 1 when there are no more characters in the receiver.

Transmit operation in mode “1”:
When the 2550 is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1), the -TXRDY pin on 44/48 pin packages will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty.

Receive operation in mode “1”:
When the 2550 is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1) and the trigger level has been reached, or a Receive Time Out has occurred, the -RXRDY pin on 44/48 pin packages will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.

FCR BIT 4-5:
Not Used - initialized to a logic 0.

FCR BIT 6-7: (logic 0 or cleared is the default condition, RX trigger level = 1)
These bits are used to set the trigger level for the receive FIFO interrupt.

An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However the FIFO will continue to be loaded until it is full.

BIT-7	BIT-6	RX FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

Interrupt Status Register (ISR)

The 2550 provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 6 (below) shows the data values (bits 0-3) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels:

Table 6, INTERRUPT SOURCE TABLE

Priority Level	[ISR BITS] Bit-3	Bit-2	Bit-1	Bit-0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
Logic 1 = No interrupt pending. (normal default condition)

ISR BIT 1-3: (logic 0 or cleared is the default condition)
These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

ISR BIT 4-5: (logic 0 or cleared is the default condition)
Not Used - initialized to a logic 0.

ISR BIT 6-7: (logic 0 or cleared is the default condition)
These bits are set to a logic 0 when the FIFO's are not being used in the 16C450 mode. They are set to a logic 1 when the FIFO's are enabled in the ST16C2550 mode.

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR BIT 0-1: (logic 0 or cleared is the default condition)
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: (logic 0 or cleared is the default condition)
The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	Word length	Stop bit length (Bit time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
Logic 0 = No parity. (normal default condition)
Logic 1 = A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.

LCR BIT-4:
If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.
Logic 0 = ODD Parity is generated by forcing an odd

number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)
Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted. The receiver must be programmed to check the same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = logic 0, parity is not forced. (normal default condition)
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

LCR Bit-5	LCR Bit-4	LCR Bit-3	Parity selection
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity "1"
1	1	1	Forced parity "0"

LCR BIT-6:
When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.
Logic 0 = No TX break condition. (normal default condition)
Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:
The internal baud rate counter latch and Enhance Feature mode enable.
Logic 0 = Divisor latch disabled. (normal default condition)
Logic 1 = Divisor latch and enhanced feature register enabled.

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:
Logic 0 = Force -DTR output to a logic 1. (normal default condition)
Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:
Logic 0 = Force -RTS output to a logic 1. (normal default condition)
Logic 1 = Force -RTS output to a logic 0.

MCR BIT-2:
This bit is used in the Loop-back mode only. In the loop-back mode this bit is use to write the state of the modem -RI interface signal.

*MCR BIT-3: (*Used to control the modem -CD signal in the loop-back mode.)
Logic 0 = Forces INT (A-B) outputs to the three state mode and sets -OP2 to a logic 1. (normal default condition)
In the Loop-back mode, sets -CD internally to a logic 1.
Logic 1 = Forces the INT (A-B) outputs to the active mode and sets -OP2 to a logic 0.
In the Loop-back mode, sets -CD internally to a logic 0.

MCR BIT-4:
Enable the local loop-back mode (diagnostics). In this mode the transmitter output (-TX) and the receiver input (-RX), -CTS, -DSR, -CD, and -RI are disconnected from the 2550 I/O pins. Internally the modem data and control pins are connected into a loop-back data configuration. In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register.

Logic 0 = Disable loop-back mode. (normal default condition)
Logic 1 = Enable local loop-back mode (diagnostics).

MCR BIT 5-7:
Not Used - initialized to a logic 0.

Line Status Register (LSR)

This register provides the status of data transfers between. the 2550 and the CPU.

LSR BIT-0:
Logic 0 = No data in receive holding register or FIFO. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR BIT-1:
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR BIT-2:
Logic 0 = No parity error. (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR BIT-3:
Logic 0 = No framing error. (normal default condition)
Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
Logic 0 = No break condition. (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR BIT-5:
This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

LSR BIT-6:
This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR BIT-7:
Logic 0 = No Error. (normal default condition)
Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the 2550 is connected to. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

MSR BIT-0:
Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the 2550 has changed state since the last time it was read. A modem Status

Interrupt will be generated.

MSR BIT-1:
Logic 0 = No -DSR Change. (normal default condition)
Logic 1 = The -DSR input to the 2550 has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:
Logic 0 = No -RI Change. (normal default condition)
Logic 1 = The -RI input to the 2550 has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:
Logic 0 = No -CD Change. (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:
During normal operation, this bit is the compliment of the -CTS input. During the loop-back mode this bit is equivalent to MCR bit-1 (-RTS).

MSR BIT-5:
During normal operation, this bit is the compliment of the -DSR input. During the loop-back mode, this bit is equivalent to MCR bit-0 (-DTR).

MSR BIT-6:
During normal operation, this bit is the compliment of the -RI input. Reading this bit in the loop-back mode produces the state of MCR bit-2 (-OP1)

MSR BIT-7:
During normal operation, this bit is the compliment of the -CD input. Reading this bit in the loop-back mode produces the state of MCR bit-3 (-OP2).

Note: Whenever any MSR bit 0-3: is set to logic “1”, a MODEM Status Interrupt will be generated.

Scratchpad Register (SPR)

The ST16C2550 provides a temporary data register to store 8 bits of user information.

ST16C2550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
-OP2	High
-RTS	High
-DTR	High
INT	Three state mode

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3 Min	Limits 3.3 Max	Limits 5.0 Min	Limits 5.0 Max	Units	Conditions
T_{1w},T_{2w}	Clock pulse duration	17		17		ns	
T_{3w}	Oscillator/Clock frequency		8		24	MHz	
T_{6s}	Address setup time	5		0		ns	
T_{7d}	-IOR delay from chip select	10		10		ns	
T_{7w}	-IOR strobe width	35		25		ns	
T_{7h}	Chip select hold time from -IOR	0		0		ns	
T_{9d}	Read cycle delay	40		30		ns	
T_{12d}	Delay from -IOR to data		35		25	ns	
T_{12h}	Data disable time		25		15	ns	
T_{13d}	-IOW delay from chip select	10		10		ns	
T_{13w}	-IOW strobe width	40		25		ns	
T_{13h}	Chip select hold time from -IOW	0		0		ns	
T_{15d}	Write cycle delay	40		30		ns	
T_{16s}	Data setup time	20		15		ns	
T_{16h}	Data hold time	5		5		ns	
T_{17d}	Delay from -IOW to output		50		40	ns	100 pF load
T_{18d}	Delay to set interrupt from MODEM input		40		35	ns	100 pF load
T_{19d}	Delay to reset interrupt from -IOR		40		35	ns	100 pF load
T_{20d}	Delay from stop to set interrupt		1		1	Rclk	
T_{21d}	Delay from -IOR to reset interrupt		45		40	ns	100 pF load
T_{22d}	Delay from stop to interrupt		45		40	ns	
T_{23d}	Delay from initial INT reset to transmit start	8	24	8	24	Rclk	
T_{24d}	Delay from -IOW to reset interrupt		45		40	ns	
T_{25d}	Delay from stop to set -RxRdy		1		1	Rclk	
T_{26d}	Delay from -IOR to reset -RxRdy		45		40	ns	
T_{27d}	Delay from -IOW to set -TxRdy		45		40	ns	
T_{28d}	Delay from start to reset -TxRdy		8		8	Rclk	
T_R	Reset pulse width	40		40		ns	
N	Baud rate devisor	1	2^{16}-1	1	2^{16}-1	Rclk	

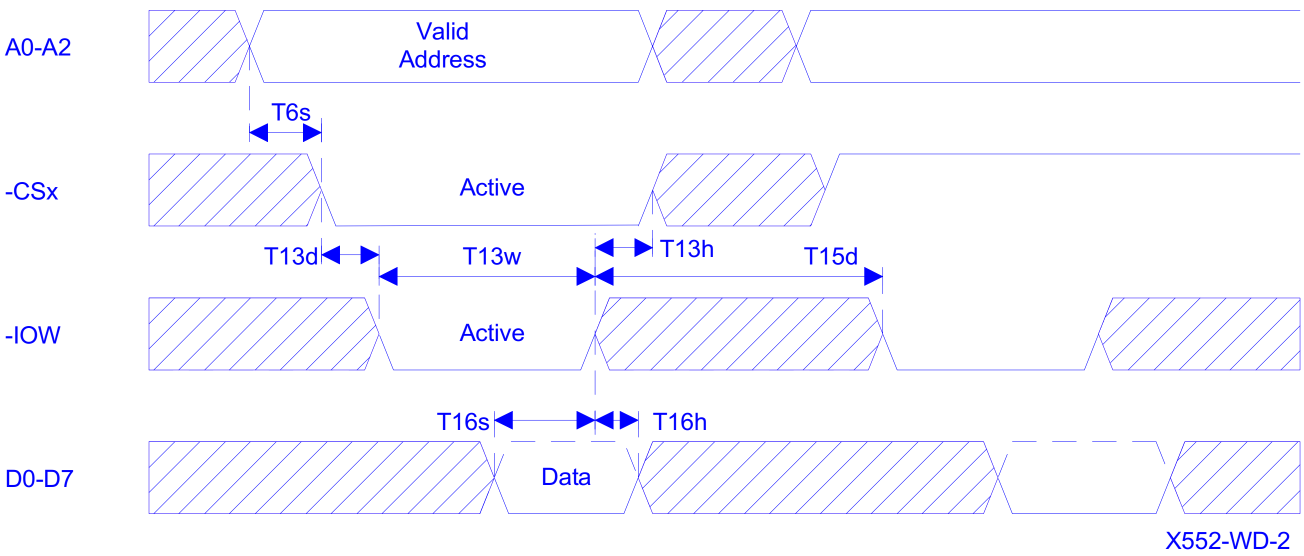
ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW

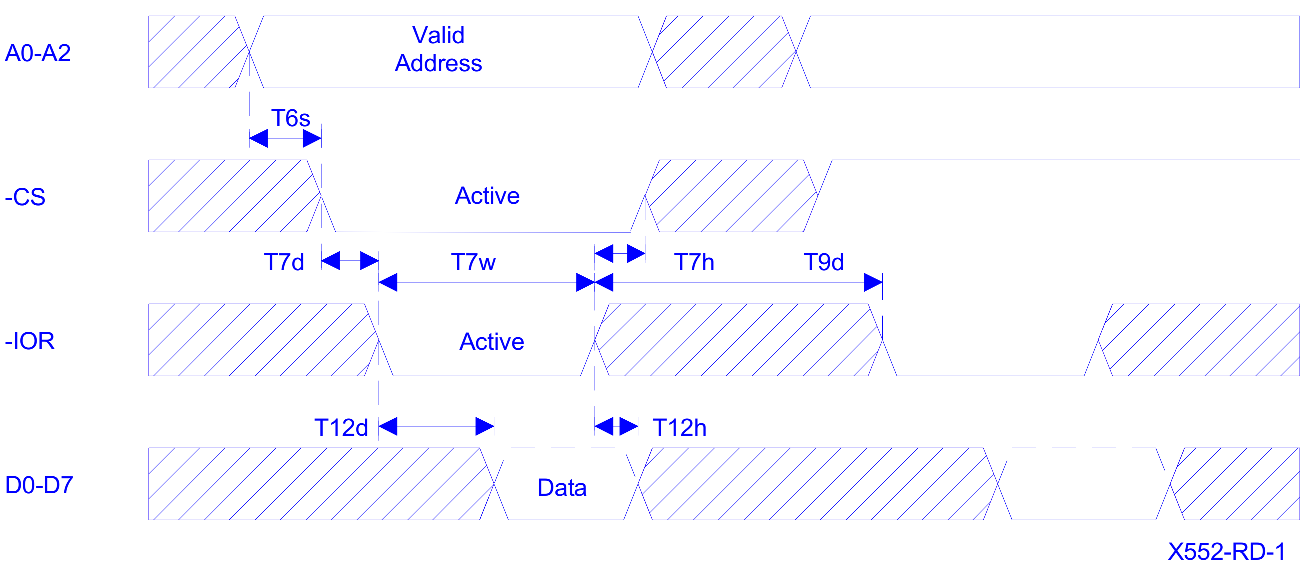
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

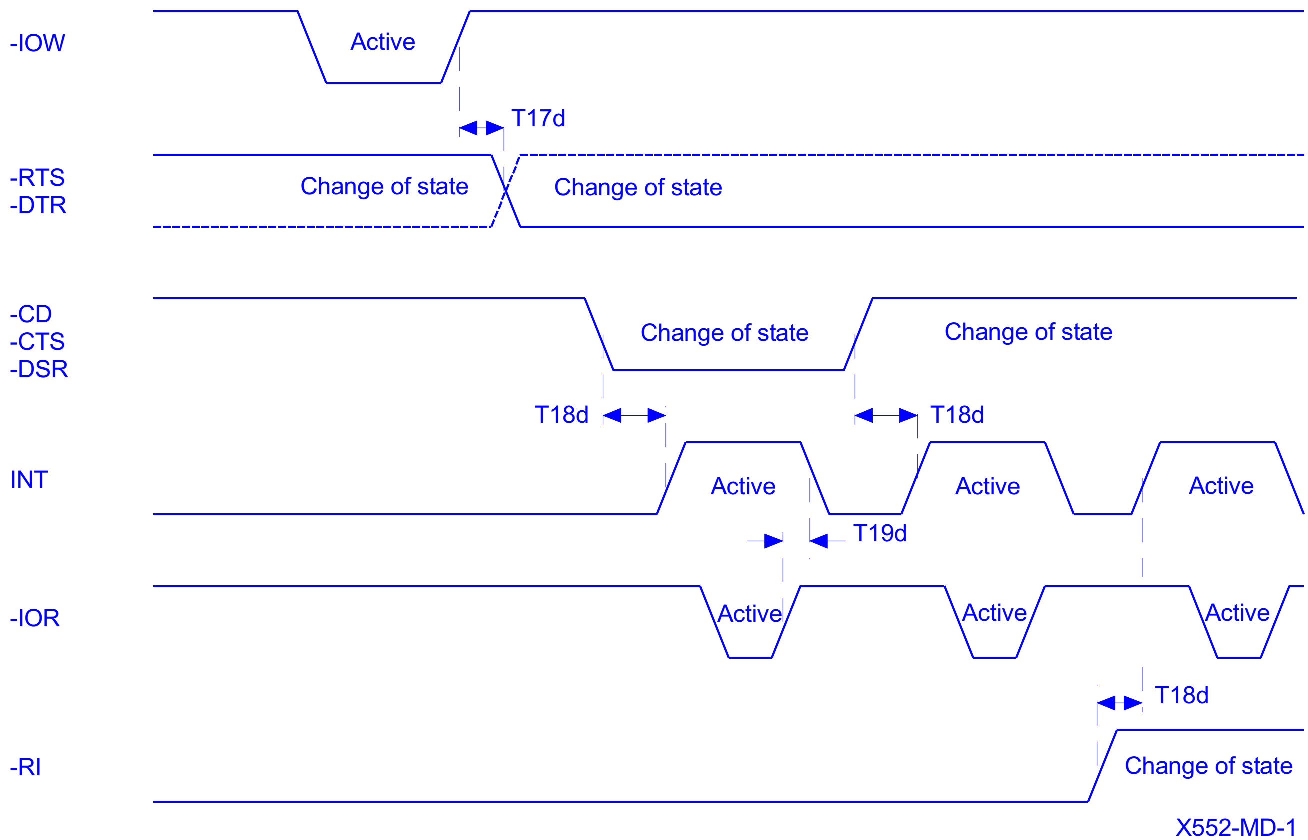
Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V_{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock input high level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input high level	2.0		2.2	VCC	V	
V_{OL}	Output low level on all outputs				0.4	V	I_{OL}= 5 mA
V_{OL}	Output low level on all outputs		0.4			V	I_{OL}= 4 mA
V_{OH}	Output high level			2.4		V	I_{OH}= -5 mA
V_{OH}	Output high level	2.0				V	I_{OH}= -1 mA
I_{IL}	Input leakage		±10		±10	µA	
I_{CL}	Clock leakage		±10		±10	µA	
I_{CC}	Avg power supply current		1.3		3	mA	
C_P	Input capacitance		5		5	pF	



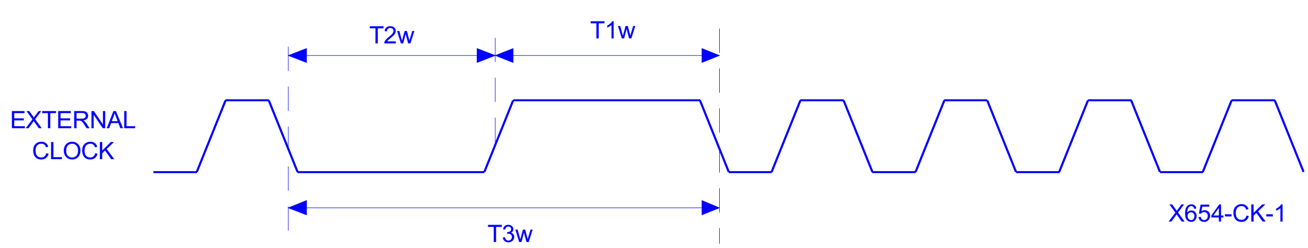
General write timing



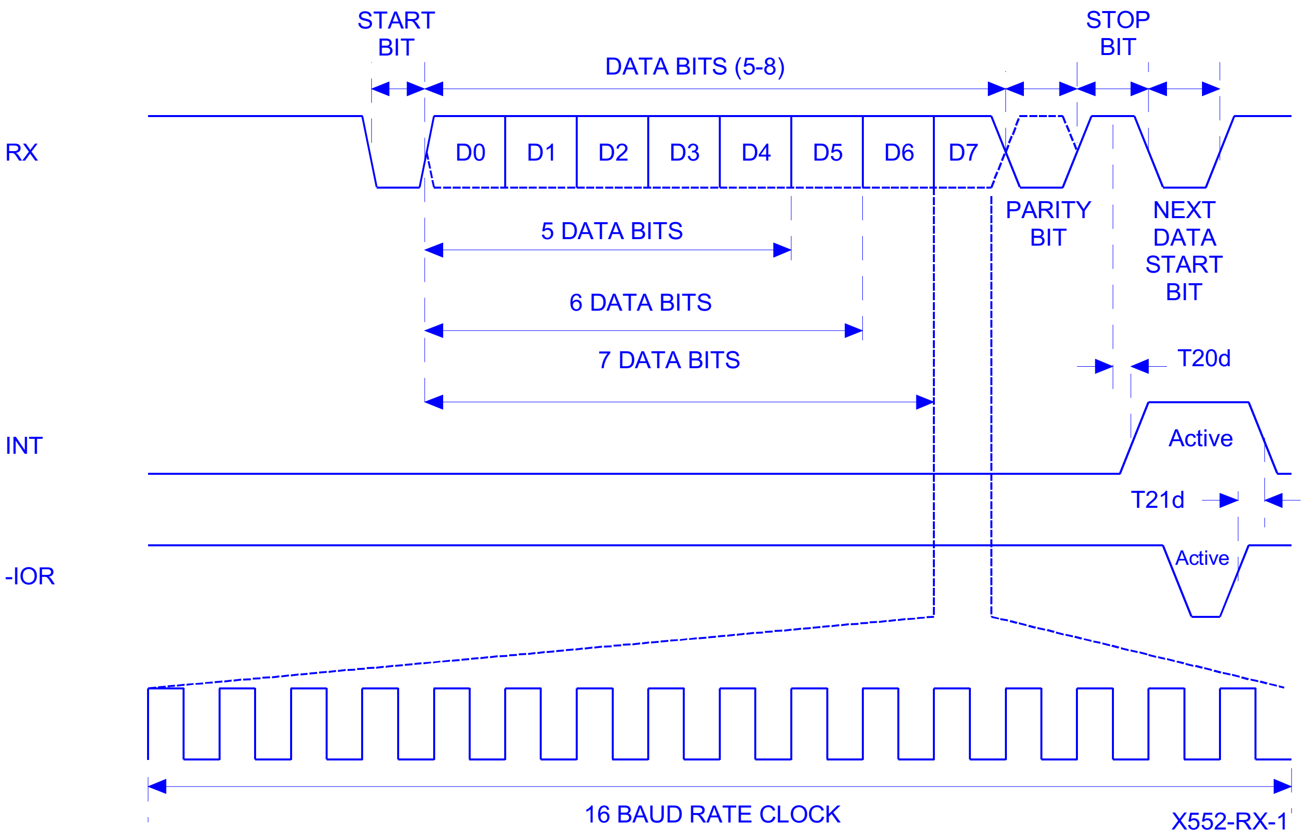
General read timing



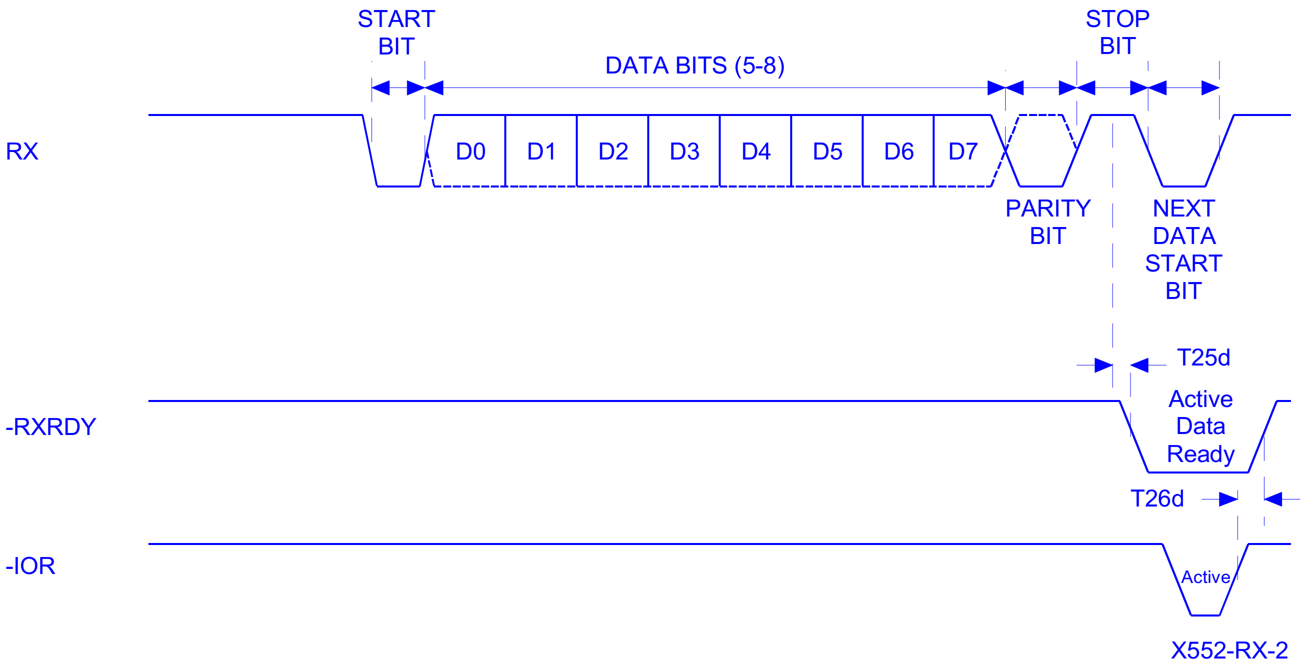
Modem input/output timing



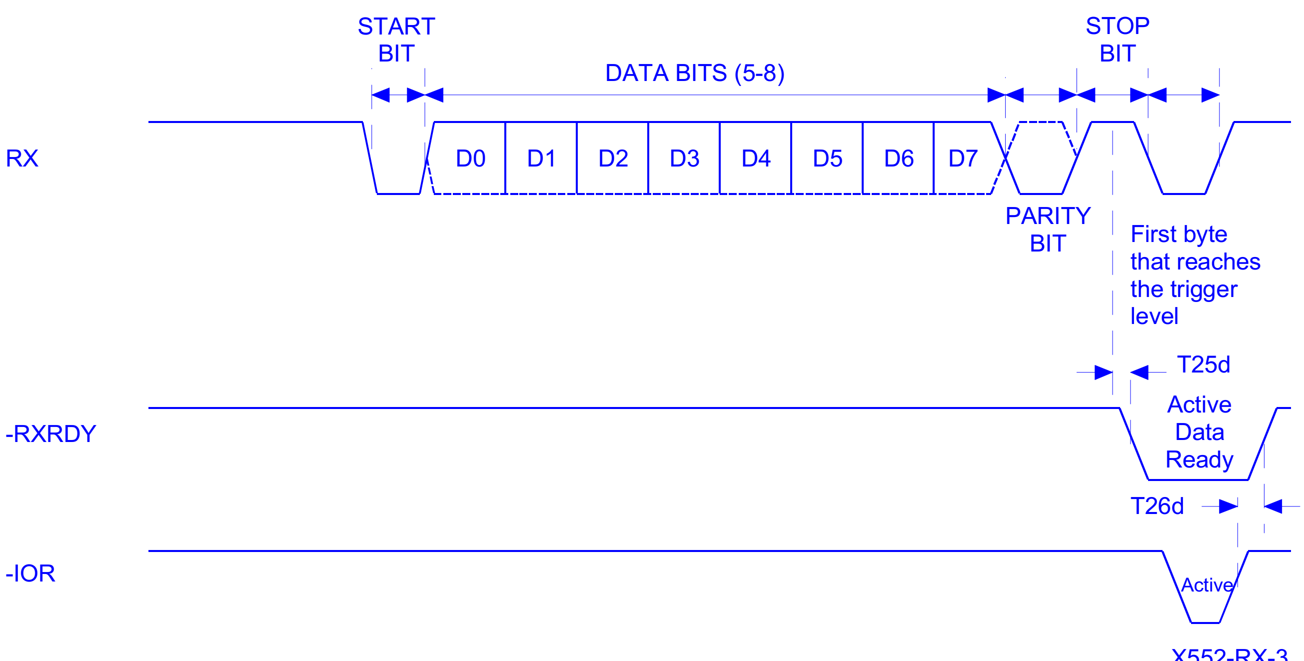
External clock timing



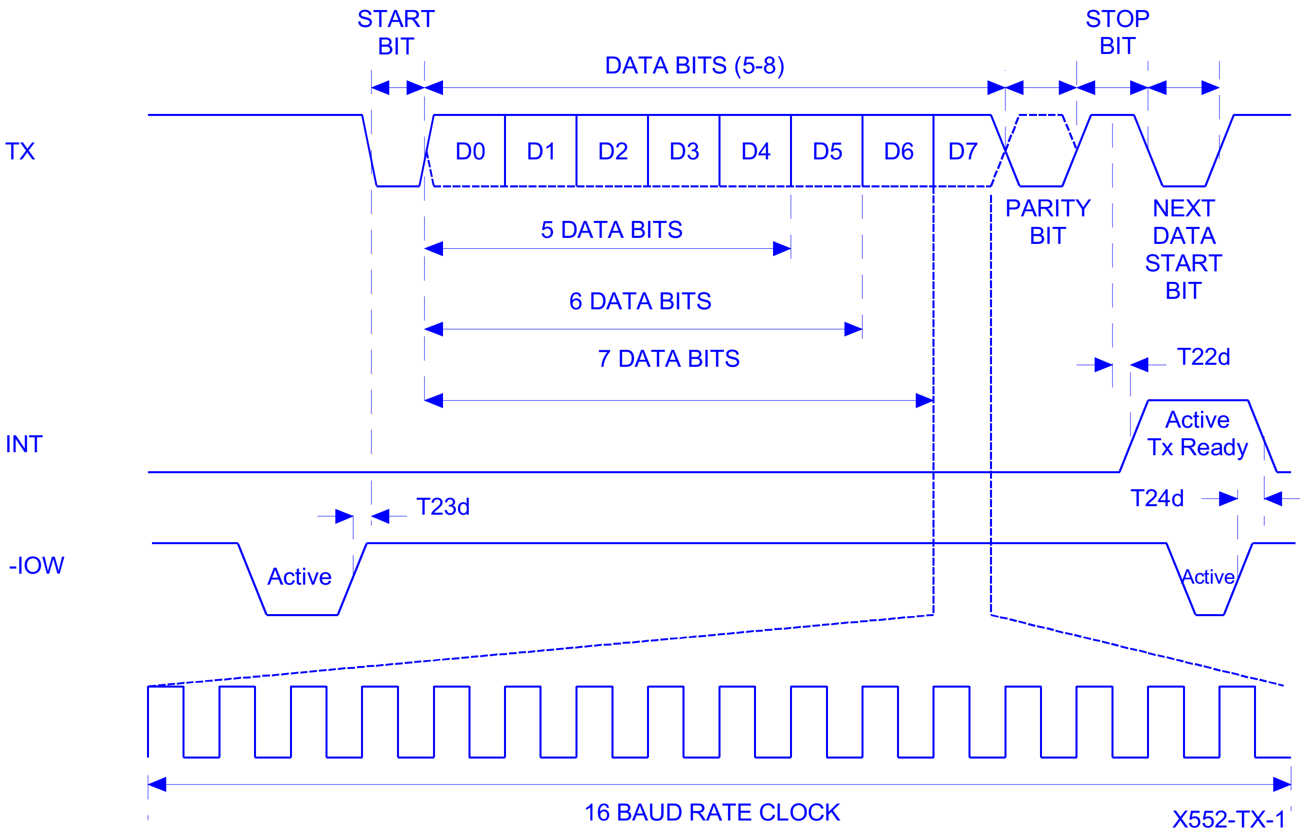
Receive timing



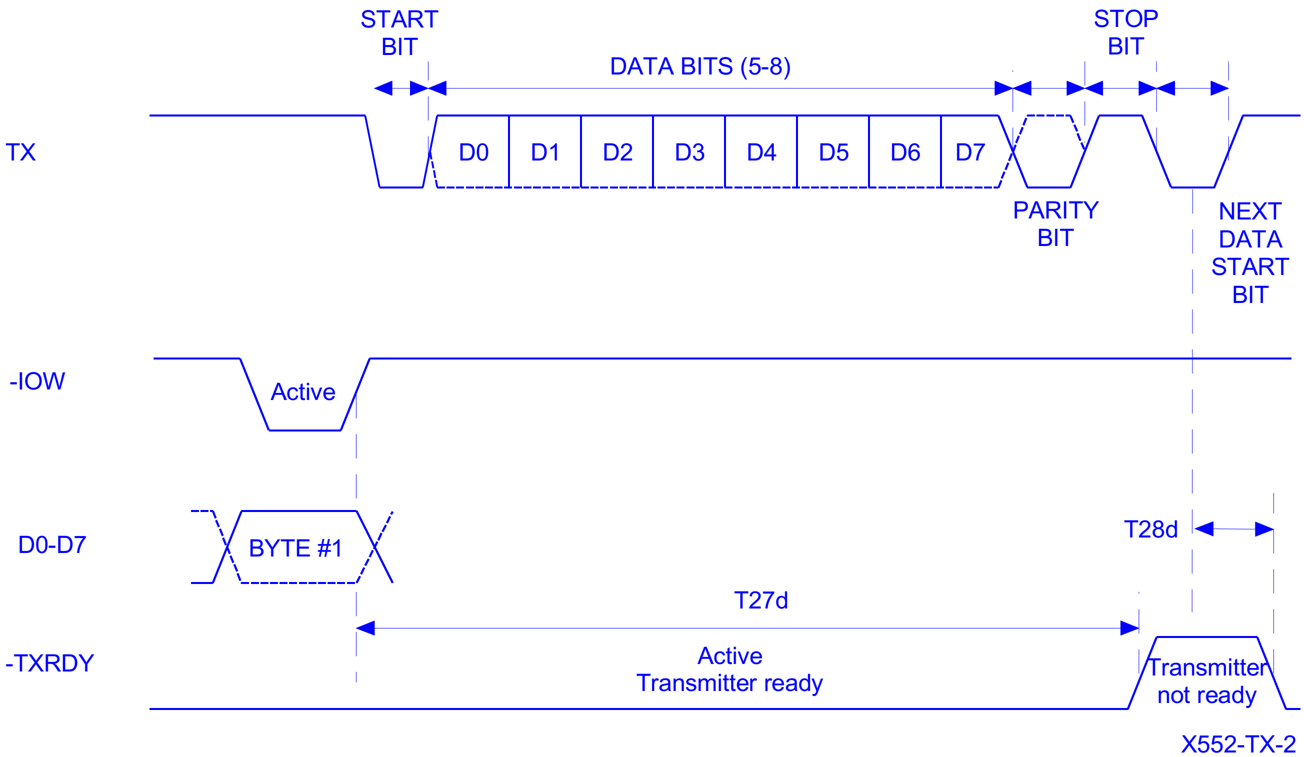
Receive ready timing in none FIFO mode



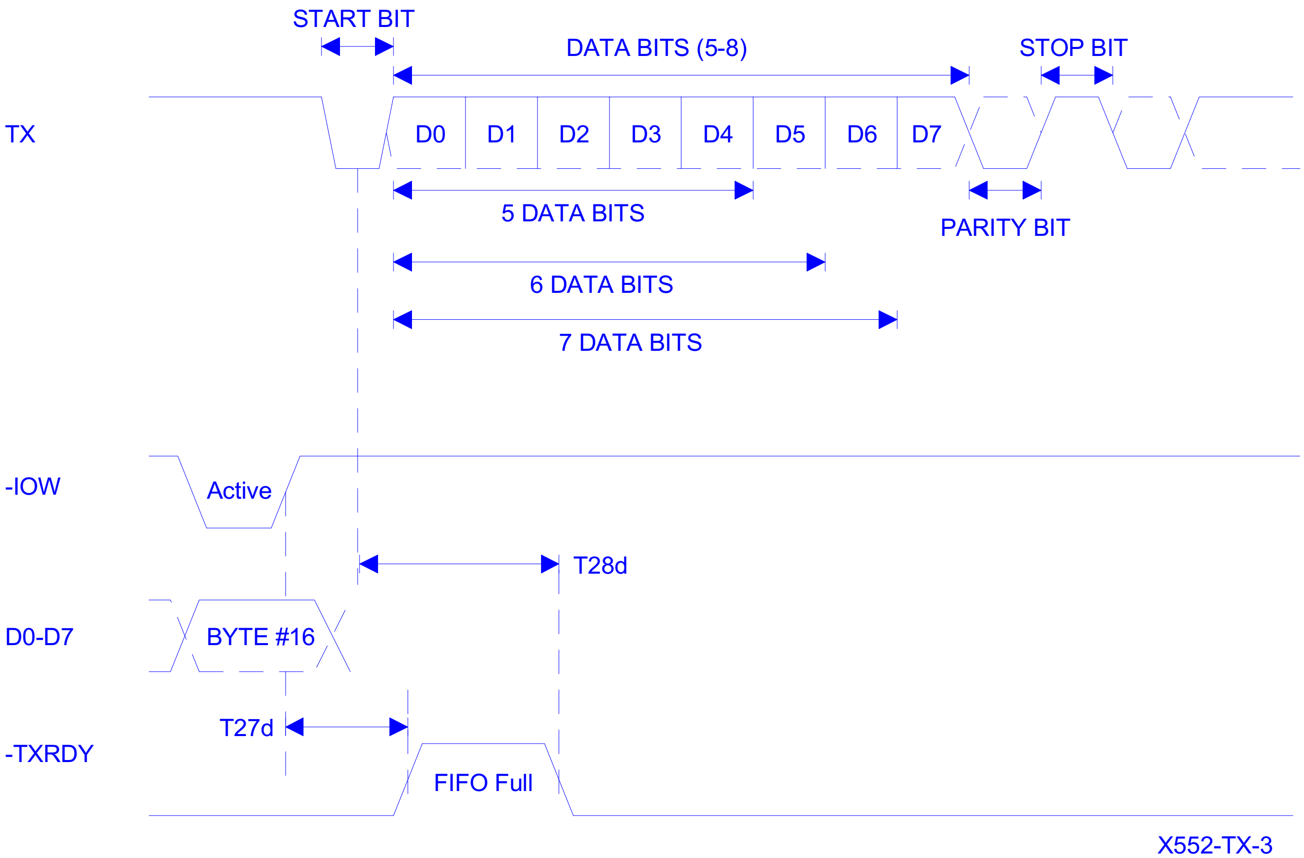
Receive timing in FIFO mode



Transmit timing



Transmit ready timing in none FIFO mode

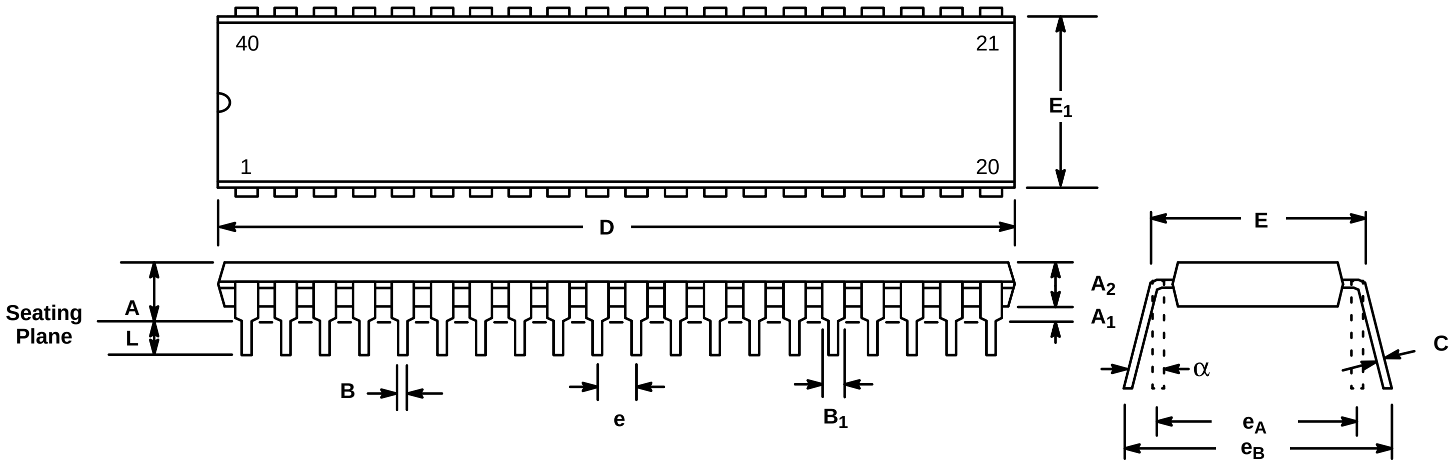


Transmit ready timing in FIFO mode

Package Dimensions

40 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)

Rev. 1.00



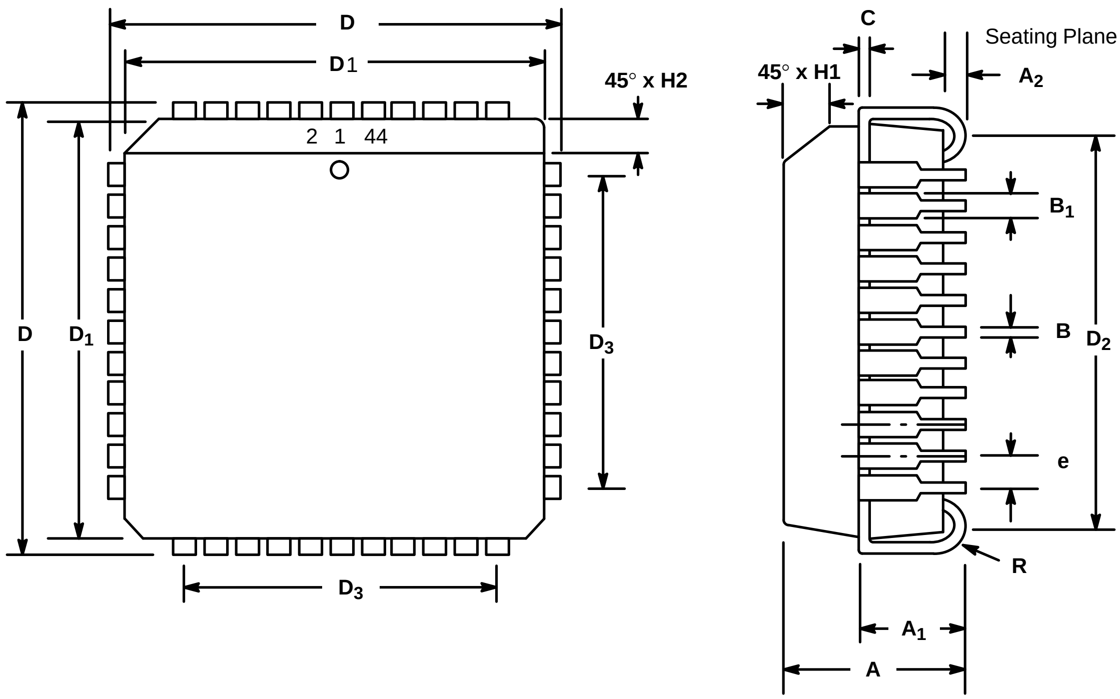
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.250	4.06	6.35
A_1	0.015	0.070	0.38	1.78
A_2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.980	2.095	50.29	53.21
E	0.600	0.625	15.24	15.88
E_1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

Package Dimensions

44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00



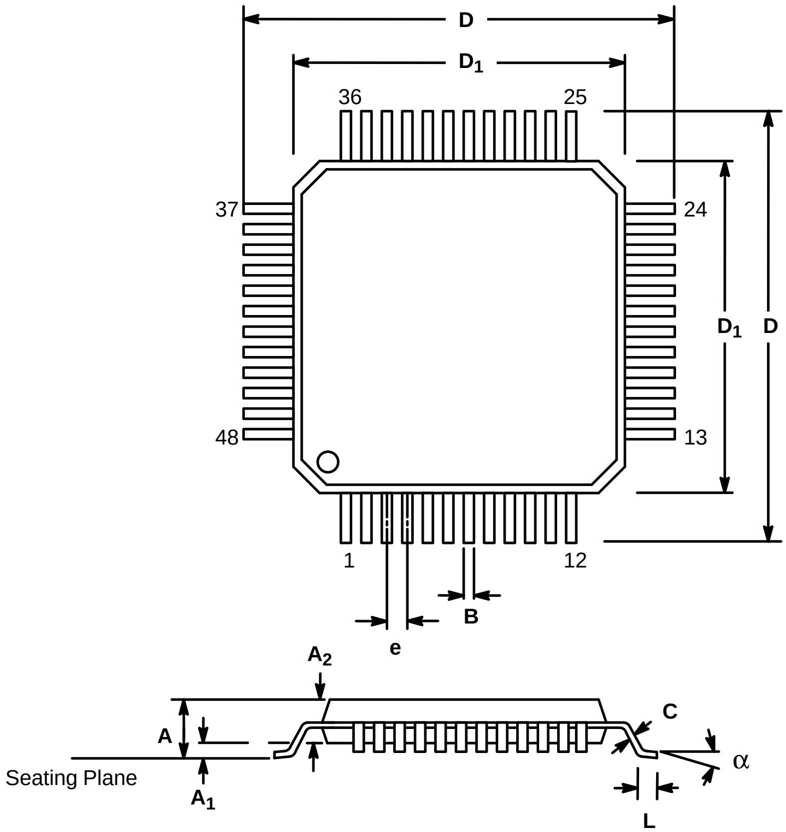
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	—.	0.51	—
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

Package Dimensions

48 LEAD THIN QUAD FLAT PACK (7 x 7 x 1.0 mm, TQFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

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