FAIRCHILD SEMICONDUCTOR™

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74ABT2952
Octal Registered Transceiver

General Description

The ABT2952 is an octal registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The output pins are guaranteed to source 32 mA and to sink 64 mA.

Features

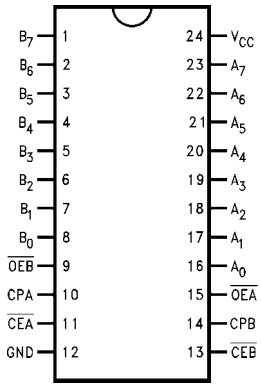
- Separate clock, clock enable and 3-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT2952CSC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT2952CMSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT2952CMTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
A_0–A_7	A-Register Inputs/B-Register 3-STATE Outputs
B_0–B_7	B-Register Inputs/A-Register 3-STATE Outputs
$\overline{OEA}$	Output Enable A-Register
CPA	A-Register Clock
$\overline{CEA}$	A-Register Clock Enable
$\overline{OEB}$	Output Enable B-Register
CPB	B-Register Clock
$\overline{CEB}$	B-Register Clock Enable

Truth Table

Output Control

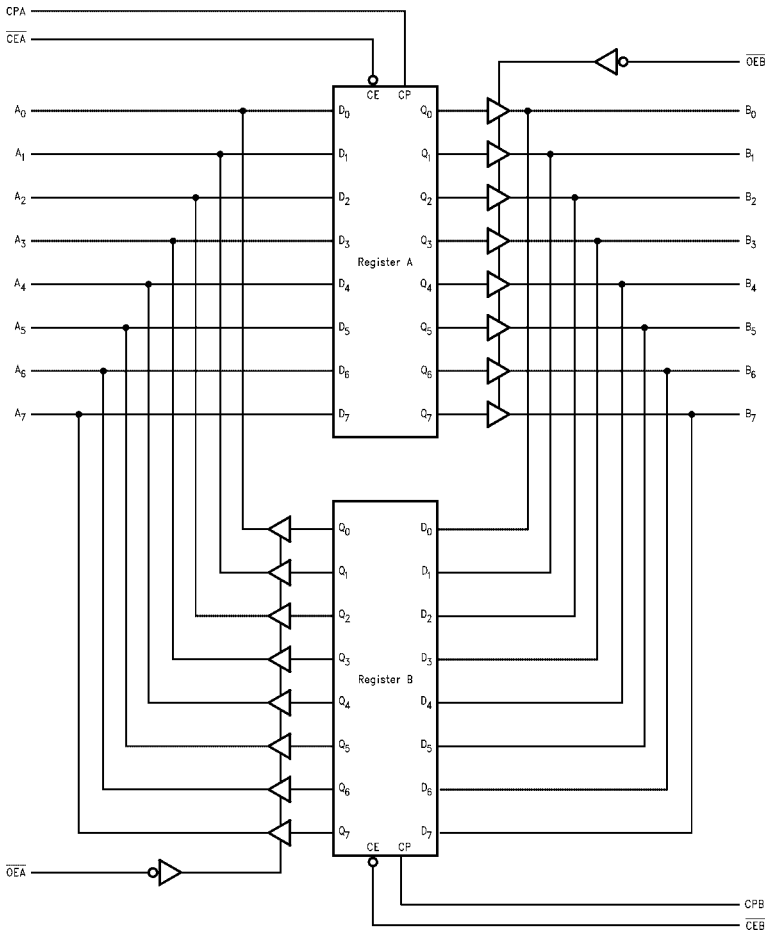
$\overline{OE}$	Internal Q	Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Register Function Table (Applies to A or B Register)

Inputs			Internal	Function
D	CP	$\overline{CE}$	Q	
X	X	H	NC	Hold Data
L	⌐	L	L	Load Data
H	⌐	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5					I_{OH} = −3 mA (A_n, B_n)
		2.0					I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			1	μA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 3)
				1			V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−1	μA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 3)
				−1			V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			10	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−10	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			250	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs 3-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V; All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 4)			0.18	mA/MHz	Max	Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND, Non-I/O = GND or V_{CC} One Bit toggling, 50% duty cycle (Note 4)

Note 3: Guaranteed, but not tested.

Note 4: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

DC Electrical Characteristics

(SOIC Package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	T_A = 25°C (Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.0		V	5.0	T_A = 25°C (Note 5)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 6)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 7)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 7)

Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

Note 7: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

(SOIC and SSOP Package)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	200			200		MHz
t_{PLH}	Propagation Delay	1.5	3.4	5.3	1.5	5.3	ns
t_{PHL}	CPA or CPB to	1.5	3.6	5.3	1.5	5.3	
	A_n or B_n						
t_{PZH}	Output Enable Time	1.5	3.2	5.5	1.5	5.5	ns
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to	1.5	3.5	5.5	1.5	5.5	
	A_n or B_n						
t_{PHZ}	Output Disable Time	1.5	3.6	6.0	1.5	6.0	ns
t_{PLZ}	$\overline{OEA}$ or $\overline{OEB}$ to	1.5	3.2	6.0	1.5	6.0	
	A_n or B_n						

AC Operating Requirements

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Max	Min	Max	
t_S(H)	Setup Time, HIGH	2.5		2.5		ns
t_S(L)	or LOW A_n or B_n	2.5		2.5		
	to CPA or CPB					
t_H(H)	Hold Time, HIGH	1.5		1.5		ns
t_H(L)	or LOW A_n or B_n	1.5		1.5		
	to CPA or CPB					
t_S(H)	Setup Time, HIGH	2.5		2.5		ns
t_S(L)	or LOW $\overline{CEA}$ or $\overline{CEB}$	2.5		2.5		
	to CPA or CPB					
t_H(H)	Hold Time, HIGH	1.5		1.5		ns
t_H(L)	or LOW $\overline{CEA}$ or $\overline{CEB}$	1.5		1.5		
	to CPA or CPB					
t_W(H)	Pulse Width,	3.0		3.0		ns
t_W(L)	HIGH or LOW	3.0		3.0		
	CPA or CPB					

Extended AC Electrical Characteristics

(SOIC Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 8)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 9)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 10)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	6.0	2.0	8.0	2.5	10.5	ns
t_{PHL}	CPA or CPB to A_n or B_n	1.5	6.0	2.0	8.0	2.5	10.5	
t_{PZH}	Output Enable Time	1.5	6.0	2.0	8.0	2.5	11.5	ns
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	6.0	2.0	8.0	2.5	11.5	
t_{PHZ}	Output Disable Time	1.5	6.0	(Note 11)		(Note 11)		ns
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	6.0					

Note 8: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 9: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 10: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 11: The 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew

(SOIC Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 12)	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 13)	Units
		Max	Max	
t_{OSHL} (Note 14)	Pin to Pin Skew HL Transitions	1.0	1.5	ns
t_{OSLH} (Note 14)	Pin to Pin Skew LH Transitions	1.0	2.0	ns
t_{PS} (Note 15)	Duty Cycle LH–HL Skew	2.0	4.5	ns
t_{OST} (Note 14)	Pin to Pin Skew LH/HL Transitions	2.1	4.5	ns
t_{PV} (Note 16)	Device to Device Skew LH/HL Transitions	2.5	5.0	ns

Note 12: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 13: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). This specification is guaranteed but not tested.

Note 15: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

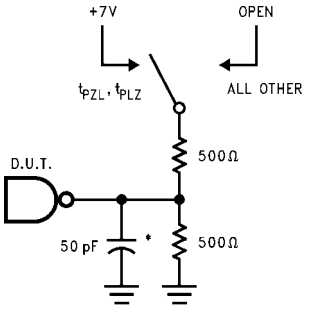
Note 16: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ (Non I/O Pins)
$C_{I/O}$ (Note 17)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 17: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

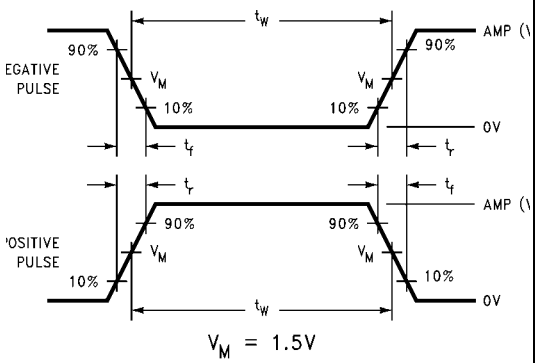


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Input Signal Requirements

AC Waveforms

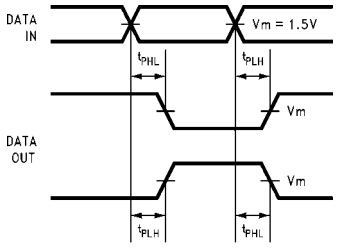


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

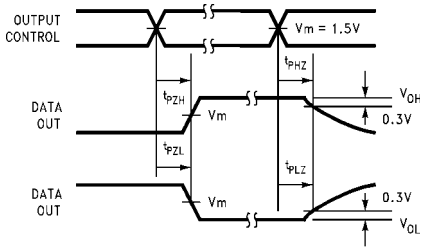


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

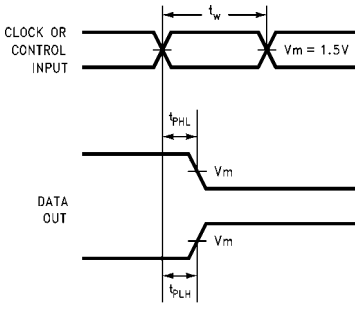


FIGURE 5. Propagation Delay, Pulse Width Waveforms

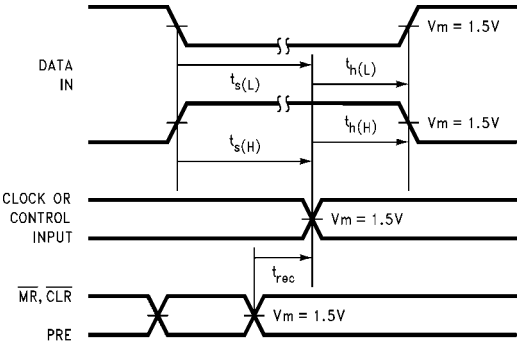
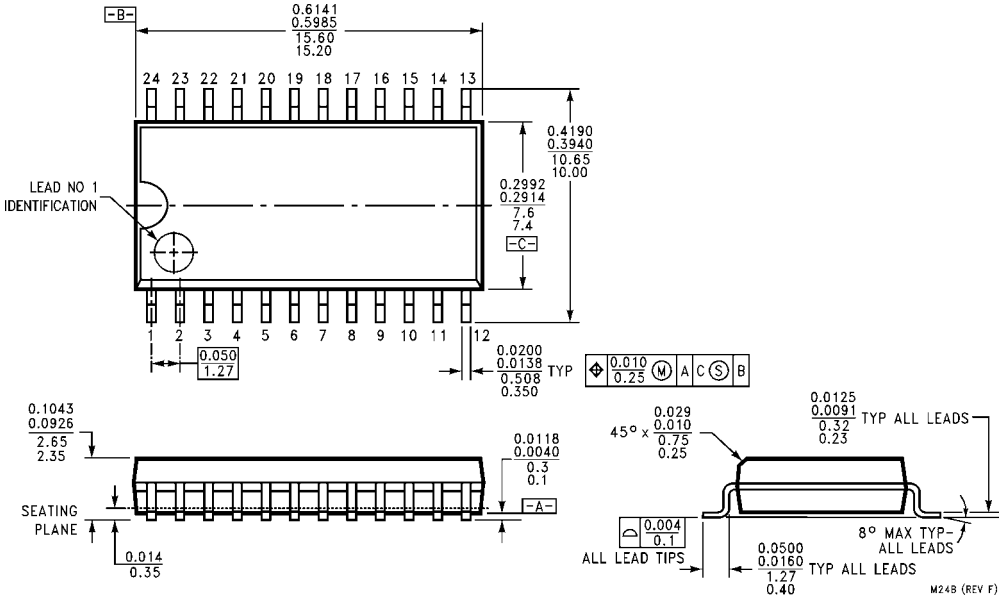
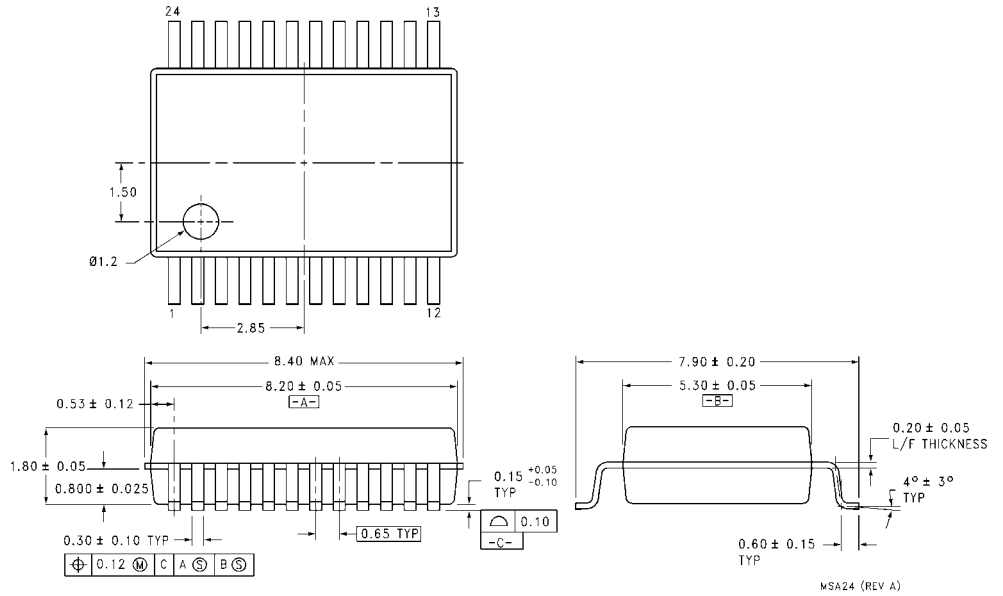


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

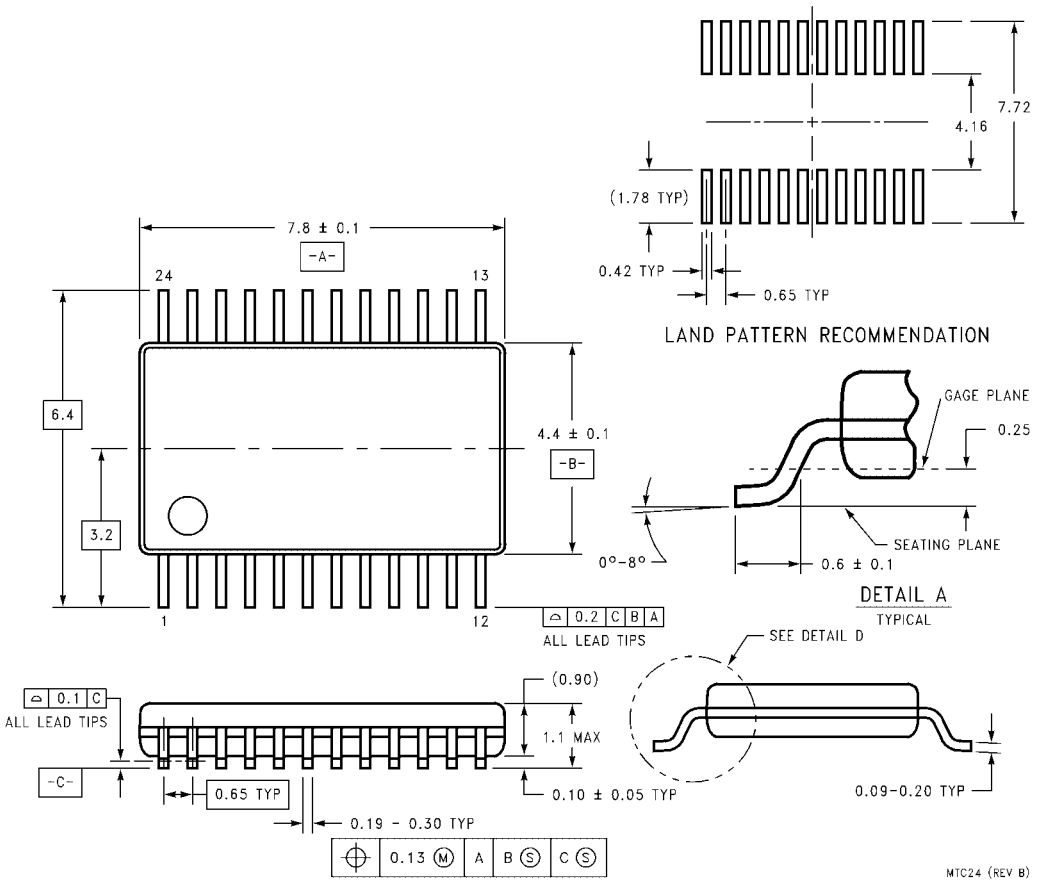


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M24B



24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24